Synthesizer Design for Microwave Applications

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ABSTRACT

The following is an introduction into the PLL basics; specifically, into such items as single- and multiloop synthesizers, including the use of fractional-division and direct digital synthesizers. We will look at the advantages and disadvantages of the various systems. Probably the most critical parameter in a synthesizer is its phase-noise performance; therefore, we are going to look at the various noise contributions within a synthesizer, and finally into its resulting overall phase noise. Some of the various approaches provide less phase noise than others; they will be discussed.

1 INTRODUCTION TO LOOP BASICS

The traditional synthesizer consists of a single loop and the step size of the output frequency is equal to the reference frequency at the phase detector. Figure 1 shows this classic approach.

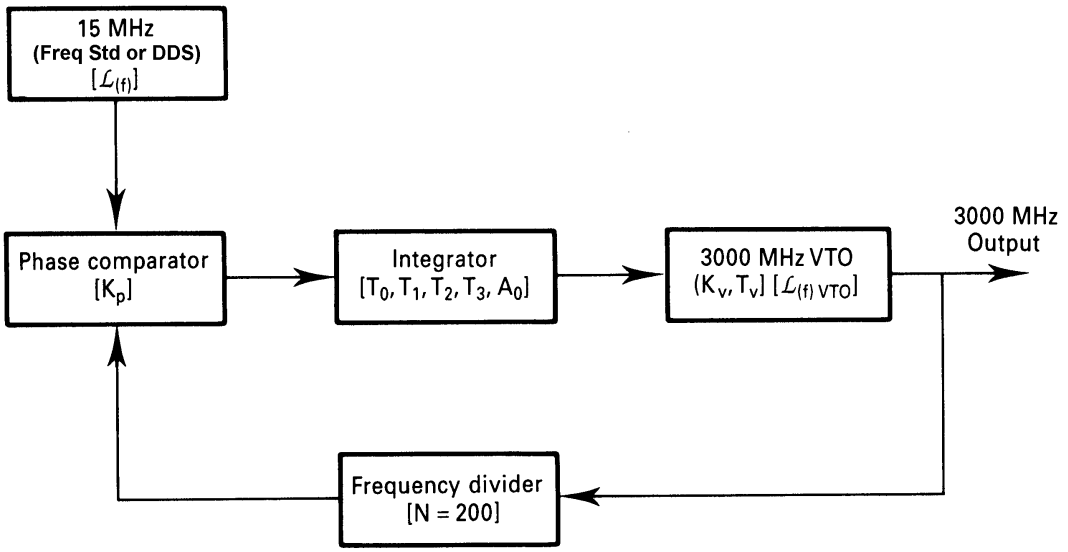

Figure 1--Block diagram of a PLL synthesizer driven by a frequency standard, DDS, or fractional-*N* synthesizer for high resolution at the output. The last two standards allow a relatively low division ratio and provide quasi-arbitrary resolution.

Wireless applications with a step size of 200 kHz have made the life of the designers somewhat easier, since such a wide step size reduces the division ratio. As can be seen in Figure 1, the simplest form of a digital synthesizer consists of a voltage-controlled oscillator (VCO). My previous presentation on oscillators has given insights into the VCO design. For PLL applications, and besides the noise performance, the oscillator sensitivity, typically expressed in

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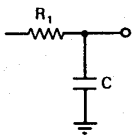
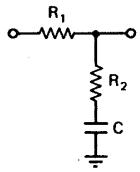
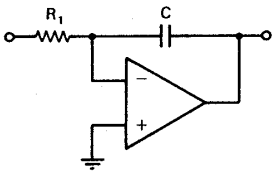
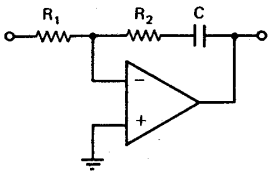
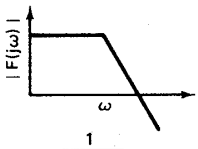
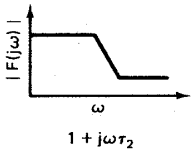
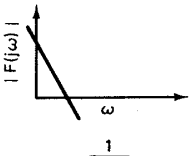
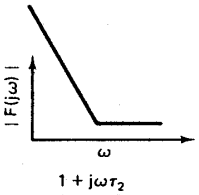
megahertz per volt (MHz/V), needs to be stated. For high-performance test equipment applications, the VCO is frequently provided in the form of a YIG oscillator. These oscillators operate at extremely high *Q* and are fairly expensive. The VCO needs to be separated from any load by a post amplifier, which drives a sine-wave-to-logic-waveform translator.

Typically, an ECL line receiver or its equivalent would serve for this function. This stage, in turn, drives a programmable divider and divides the oscillator frequency down to a reference frequency such as 200 kHz as an example. Assuming an oscillator frequency of 1 GHz, the division ratio would be 1 GHz/200 kHz = 5000. We will address this issue later. In Figure 1, however, we are looking at a 3 GHz output frequency and a step size determined by the reference source resolution, assuming a fixed division ratio.

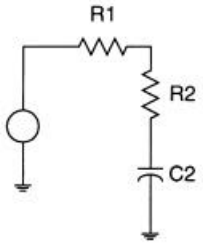
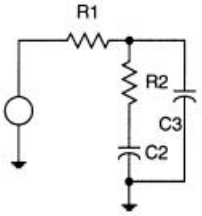
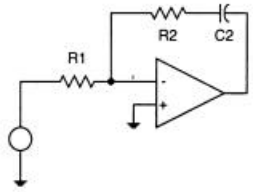
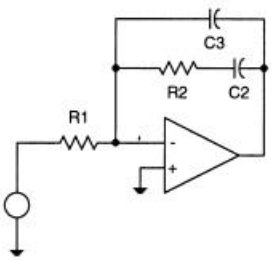
The phase detector, actually the phase/frequency detector (PFD), is driven by the reference frequency on one side and the oscillator frequency, divided down, on the other side. The PFD is typically designed to operate from a few kilohertz to several tens of megahertz, such as 50 MHz as an example. In our case, this would mean a step size of 50 MHz. Most of these phase detectors are using MOS technology to keep the levels for ON/OFF voltage high, and their noise contribution needs to be carefully evaluated. While the synthesizer is not locked, the output of the PFD is a dc control voltage with a superimposed ac voltage equal to the difference between the two frequencies prior to lock. Most PFDs have a flip-flop-based architecture, and their output consists of a train of pulses that must to be integrated to produce the control voltage necessary for driving the VCO into the locked condition. This integrator also serves as a loop filter. Its purpose is to suppress the reference frequency and provide the necessary phase/frequency response for stable locking. The basic loop really is a nonlinear control loop that, for the purpose of analysis, is always assumed to be linear or piecewise-linear. The most linear phase detector is a diode ring, but it has a low-level dc output. It requires an operational amplifier to shift the level of typically ±0.3 V to the high voltage required for the tuning diode. These values are typically somewhere between 5 and 30 V. The tuning diode itself needs to have the appropriate breakdown voltage and voltage-dependent linearity to provide constant loop gain. In most cases, this is not possible, especially if the division ratio changes by a factor of 2 or more; in this case, it is a wise decision to use coarse steering so that fine tuning shows a reasonably linear performance. These loops are also called Type 2 second-order loops. This is due to the fact that the loop has two integrators, one being the loop filter and other one being the tuning diode. The order of the loop is determined by the filter. Table 1 shows circuit and transfer characteristics of several PLL filters.

Table 1--Circuit and Transfer Characteristics of Several PLL Filters

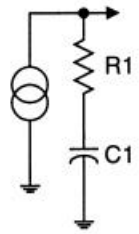
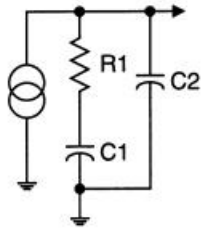
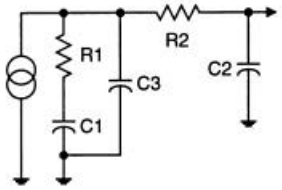
Type	Passive		Active	
	1	2	3	4
Circuit				
Transfer characteristic				
$F(j\omega) =$	$\frac{1}{1+j\omega\tau_1}$	$\frac{1+j\omega\tau_2}{1+j\omega(\tau_1+\tau_2)}$	$\frac{1}{j\omega\tau_1}$	$\frac{1+j\omega\tau_2}{j\omega\tau_1}$

$\tau_1 = R_1C,\ \tau_2 = R_2C$

Implementation of Different Loop Filters

Passive Lead-Lag	Passive Lead Lag with Pole	Active Integrator	Active Integrator with Pole
			
$F(s) = \frac{s\tau_2+1}{[s(\tau_1+\tau_2)+1]}$ $\tau_1 = R_1C_2; \tau_2 = R_2C_2$	$F(s) = \frac{s\tau_2+1}{[s(\tau_1+\tau_2)+1](s\tau_3+1)}$ $\tau_1 = R_1C_2; \tau_2 = R_2C_2;$ $\tau_3 = (R_2 \| R_1)C_3$	$F(s) = \frac{s\tau_2+1}{s\tau_1}$ $\tau_1 = R_1C_2; \tau_2 = R_2C_2;$	$F(s) = \frac{s\tau_2+1}{s\tau_1(s\tau_3+1)}$ $\tau_1 = R_1(C_2+C_3); \tau_2 = R_2C_2;$ $\tau_3 = R_2(C_3 \| C_2)$
Type 1.5, 2nd Order (Low Gain)	Type 1.5, 3rd Order (Low Gain)	Type 2, 2nd Order (High Gain)	Type 2, 3rd Order (High Gain)

Recommended Passive Filters for Charge Pumps

Integrator	Integrator With Poles	Integrator With 2 Poles
		
$F(s) = R_1 \frac{s\tau_1 + 1}{s\tau_1}$ $\tau_1 = R_1C_1$	$F(s) = R_1 \frac{s\tau_1 + 1}{s\tau_1(s\tau_2 + 1)}$ $\tau_1 = R_1C_1; \tau_2 = R_2(\frac{C_1C_2}{C_1 + C_2})$	$F(s) = R_1 \frac{s\tau_1 + 1}{s\tau_1(s\tau_2 + 1)(s\tau_3 + 1)}$ $\tau_1 = R_1C_1; \tau_2 = R_1 \frac{C_1C_3}{C_1 + C_3};$ $\tau_3 = R_2C_2$
Type 2, 2nd Order	Type 2, 3rd Order	Type 2, 4th Order

These filters are single-ended, which means that they are driven from the output of a CMOS switch in the phase/frequency detector. This type of configuration shows a problem under lock conditions: If we assume that the CMOS switches are identical and have no leakage, initially the output current charges the integrator and the system will go into lock. If it is locked and stays locked, there is no need for a correction voltage, and therefore the CMOS switches will not supply any output. The very moment a tiny drift occurs, a correction voltage is required, and therefore there is a drastic change from no loop gain (closed condition) to a loop gain (necessary for acquiring lock). This transition causes all kinds of nonlinear phenomena, and therefore it is a better choice to either use a passive filter in a symmetrical configuration or a symmetrical loop filter with an operational amplifier instead of the CMOS switches. Many of the modern PFDs have different outputs to accommodate this. An ill-conditioned filter or selection of values for the filter frequently leads to a very low-frequency type of oscillation, also referred to as motorboating. This can only be corrected by adjusting the phase/frequency behavior of the filter.

An easy way of designing the appropriate loop filter and getting insight into the loop is using a Bode diagram. The Bode diagram shows the open-loop performance, both magnitude and phase, of the phase-locked loop. For stability, several rules apply.

1-1 The Type 2, Second-Order Loop

The following is a derivation of the properties of the Type 2, second-order loop. This means that the loop has two integrators, one being the diode and the other the operational amplifier, and is built with the order of 2 as can be seen from the pictures above. The basic principle to derive the performance for higher-order loops follows the same principle, although the derivation is more complicated. Following the math section, we will show some typical responses.

The Type 2, second-order loop uses a loop filter in the form

$$F(s) = \frac{1}{s} \frac{\tau_2 s + 1}{\tau_1} \tag{1}$$

The multiplier 1/*s* indicates a second integrator, which is generated by the active amplifier. In Table 1, this is the Type 3 filter. The Type 4 filter is mentioned there as a possible configuration but is not recommended because, as stated previously, the addition of the pole of the origin creates difficulties with loop stability and, in most cases, requires a change from the Type 4 to the Type 3 filter. One can consider the Type 4 filter as a special case of the Type 3 filter, and therefore it does not have to be treated separately. Another possible transfer function is

$$F(s) = \frac{1}{R_1 C}\frac{1+\tau_2 s}{s} \tag{2}$$

with

$$\tau_2 = R_2 C \tag{3}$$

Under these conditions, the magnitude of the transfer function is

$$|F(j\omega)| = \frac{1}{R_1 C\omega}\sqrt{1+(\omega R_2 C)^2} \tag{4}$$

and the phase is

$$\theta = \arctan(\omega\tau_2) - 90 \text{ degrees} \tag{5}$$

Again, as if for a practical case, we start off with the design values w_n and x, and we have to determine t_1 and t_2. Taking an approach similar to that for the Type 1, second-order loop, the results are

$$\tau_1 = \frac{K}{\omega_n} \tag{6}$$

and

$$\tau_2 = \frac{2\zeta}{\omega_n} \tag{7}$$

and

$$R_1 = \frac{\tau_1}{C} \tag{8}$$

and

$$R_2 = \frac{\tau_2}{C} \tag{9}$$

The closed-loop transfer function of a Type 2, second-order PLL with a perfect integrator is

$$B(s) = \frac{K(R_2/R_1)[s + (1/\tau_2)]}{s^2 + K(R_2/R_1)s + (K/\tau_2)(R_2/R_1)} \tag{10}$$

By introducing the terms x and w_n, the transfer function now becomes

$$B(s) = \frac{2\zeta\omega_n s + \omega_n^2}{s^2 + 2\zeta\omega_n s + \omega_n^2} \tag{11}$$

with the abbreviations

$$\omega_n = \left(\frac{K}{\tau_2}\frac{R_2}{R_1}\right)^{1/2} \quad \text{rad/s} \tag{12}$$

and

$$\zeta = \frac{1}{2}\left(K\tau_2\frac{R_2}{R_1}\right)^{1/2} \tag{13}$$

and $K = K_q K_o/N$.

The 3-dB bandwidth of the Type 2, second-order loop is

$$B_{3\text{dB}} = \frac{\omega_n}{2\pi}[2\zeta^2 + 1 + \sqrt{(2\zeta^2 + 1)^2 + 1}]^{1/2} \quad \text{Hz} \tag{14}$$

and the noise bandwidth is

$$B_n = \frac{K(R_2/R_1) + 1/\tau_2}{4} \quad \text{Hz} \tag{15}$$

Again, we ask the question of the final error and use the previous error function,

$$E(s) = \frac{s\theta(s)}{s + K(R_2/R_1)\{[s + (1/\tau_2)]/s\}} \tag{16}$$

or

$$E(s) = \frac{s^2\theta(s)}{s^2 + K(R_2/R_1)s + (K/\tau_2)(R_2/R_1)} \tag{17}$$

As a result of the perfect integrator, the steady-state error resulting from a step change in input

phase or change of magnitude of frequency is zero.

If the input frequency is swept with a constant range change of input frequency ($\Delta w/dt$), for $q(s) = (2\Delta w/dt)/s^3$, the steady-state phase error is

$$E(s) = \frac{R_1}{R_2}\frac{\tau_2(2\Delta\omega/dt)}{K} \quad \text{rad} \tag{18}$$

The maximum rate at which the VCO frequency can be swept for maintaining lock is

$$\frac{2\Delta\omega}{dt} = \frac{N}{2\tau_2}\left(4B_n - \frac{1}{\tau_2}\right) \quad \text{rad/s} \tag{19}$$

The introduction of N indicates that this is referred to the VCO rather than to the phase/frequency comparator. In the previous example of the Type 1, first-order loop, we referred it only to the phase/frequency comparator rather than the VCO.

Figure 2 shows the closed-loop response of a Type 2, third-order loop having a phase margin of 10° and with the optimal 45°.

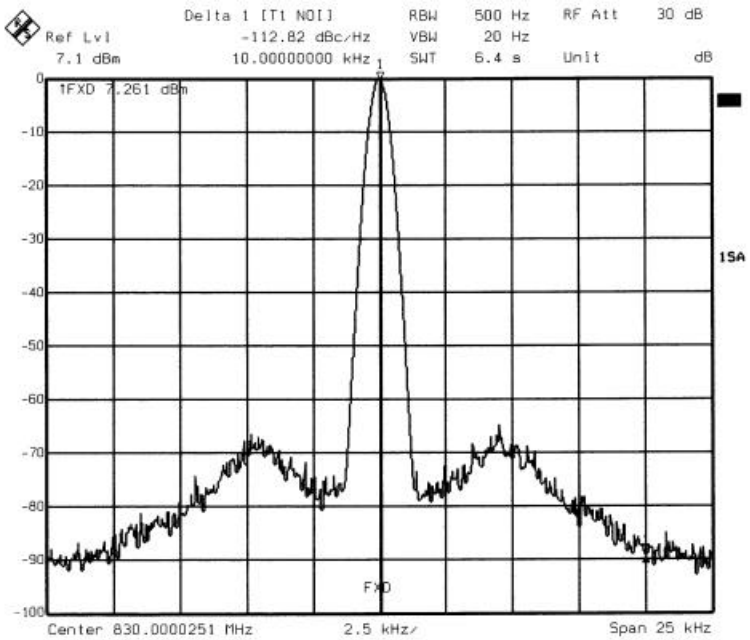


Figure 2--Measured spectrum of a synthesizer where the loop filter is underdamped, resulting in ≈10-dB increase of the phase noise at the loop-filter bandwidth. In this case, we either don't meet the 45° phase margin criterion, or the filter is too wide, so it shows the effect of the up-converted reference frequency.

A phase margin of 10° results in overshoot, which in the frequency domain would be seen as peaks in the oscillator noise-sideband spectrum. Needless to say, this is a totally undesirable effect, and since the operational amplifiers and other active and passive elements add to this, the loop filter has to be adjusted after the design is finalized to accommodate the proper resulting phase margin (35° to 45°). The open-loop gain for different loops can be seen in Figures 3 and 4.

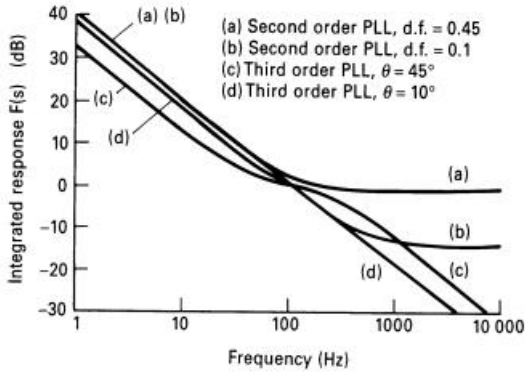


Figure 3--Integrated response for various loops as a function of the phase margin.

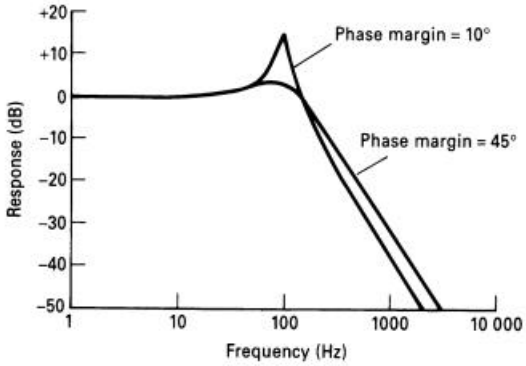
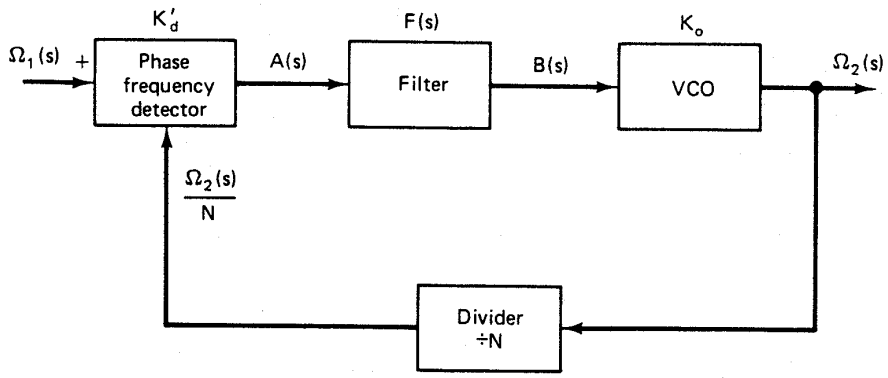


Figure 4--Closed-loop response of a Type 2, third-order PLL having a phase margin of 10°.

1-2 Transient Behavior of Digital Loops Using Tri-State Phase Detectors

Pull-In Characteristic. The Type 2, second-order loop is used with either a sample/hold comparator or a tri-state phase/frequency comparator.

We will now determine the transient behavior of this loop. Figure 5 shows the block diagram.



Note: The frequency transfer const. of the VCO = K_o
(not $\frac{K_o}{s}$, which is valid for phase transfer only.)

Figure 5--Block diagram of a digital PLL before lock is acquired.

Very rarely in the literature is a clear distinction between pull-in and lock-in characteristics or

frequency and phase acquisition made as a function of the digital phase/frequency detector. Somehow, all the approximations or linearizations refer to a sinusoidal phase/frequency comparator or its digital equivalent, the exclusive-OR gate.

The tri-state phase/frequency comparator follows slightly different mathematical principles. The phase detector gain is

$$K_d' = \frac{V_d}{\omega_0} = \frac{\text{phase detector supply voltage}}{\text{loop idling frequency}}$$

and is valid only in the out-of-lock state and is a somewhat coarse approximation to the real gain which, due to nonlinear differential equations, is very difficult to calculate. However, practical tests show that this approximation is still fairly accurate.

Definitions:

$\Omega_1(s) = \mathcal{L}[\Delta\omega_1(t)]$ Reference input to δ/ω detector

$\Omega_2(s) = \mathcal{L}[\Delta\omega_2(t)]$ Signal VCO output frequency

$\Omega_e(s) = \mathcal{L}[\omega_e(t)]$ Error frequency at δ/ω detector

$$\Omega_e(s) = \Omega_1(s) - \frac{\Omega_2(s)}{N}$$

$$\Omega_2(s) = [\Omega_1(s) - \Omega_e(s)]N$$

From the circuit above,

$$A(s) = \Omega_e(s)K_d'$$
$$B(s) = A(s)F(s)$$
$$\Omega_2(s) = B(s)K_o$$

The error frequency at the detector is

$$\Omega_e(s) = \Omega_1(s)N\frac{1}{N + K_o K_d' F(s)} \tag{20}$$

The signal is stepped in frequency:

$$\Omega_1(s) = \frac{\Delta\omega_1}{s} \quad (\Delta\omega_1 = \text{magnitude of frequency step}) \tag{21}$$

Active Filter of First Order. If we use an active filter

$$F(s) = \frac{1 + s\tau_2}{s\tau_1} \tag{22}$$

and insert this in (20), the error frequency is

$$\Omega_e(s) = \Delta\omega_1 N \frac{1}{s\left(N + K_o K_d' \frac{\tau_2}{\tau_1}\right) + \frac{K_o K_d'}{\tau_1}} \tag{23}$$

Utilizing the Laplace transformation, we obtain

$$\omega_e(t) = \Delta\omega_1 \frac{1}{1 + K_o K_d'(\tau_2/\tau_1)(1/N)} \exp\left[-\frac{t}{(\tau_1 N/K_o K_d') + \tau_2}\right] \tag{24}$$

and

$$\lim_{t\to 0} \omega_e(t) = \frac{\Delta\omega_1 N}{N + K_o K_d'(\tau_2/\tau_1)} \tag{25}$$

$$\lim_{t\to\infty} \omega_e(t) = 0 \tag{26}$$

Passive Filter of First Order. If we use a passive filter

$$\lim_{t\to\infty} \omega_e(t) = 0 \tag{27}$$

for the frequency step

$$\Omega_1(s) = \frac{\Delta\omega_1}{s} \tag{28}$$

the error frequency at the input becomes

$$\Omega_e(s) = \Delta\omega_1 N \left\{\frac{1}{s} \frac{1}{s[N(\tau_1 + \tau_2) + K_o K_d' \tau_2] + (N + K_o K_d')} + \frac{\tau_1 + \tau_2}{s[N(\tau_1 + \tau_2) + K_o K_d' \tau_2] + (N + K_o K_d')}\right\} \tag{29}$$

For the first term we will use the abbreviation *A*, and for the second term we will use the abbreviation *B*.

$$A = \frac{1/[N(\tau_1 + \tau_2) + K_o K_d' \tau_2]}{s\left[s + \frac{N + K_o K_d'}{N(\tau_1 + \tau_2) + K_o K_d' \tau_2}\right]} \tag{30}$$

$$B = \frac{\dfrac{\tau_1 + \tau_2}{N(\tau_1 + \tau_2) + K_o K'_d \tau_2}}{s + \dfrac{N + K_o K'_d}{N(\tau_1 + \tau_2) + K_o K'_d \tau_2}} \tag{31}$$

After the inverse Laplace transformation, our final result becomes

$$\mathcal{L}^{-1}(A) = \frac{1}{N + K_o K'_d}\left\{1 - \exp\left[-t\frac{N + K_o K'_d}{N(\tau_1 + \tau_2) + K_o K'_d \tau_2}\right]\right\} \tag{32}$$

$$\mathcal{L}^{-1}(B) = \frac{\tau_1 + \tau_2}{N(\tau_1 + \tau_2) + K_o K'_d \tau_2} \exp\left(-t\frac{N + K_o K'_d}{N(\tau_1 + \tau_2) + K_o K'_d \tau_2}\right) \tag{33}$$

and finally

$$\omega_e(t) = \Delta\omega_1 N[\mathcal{L}^{-1}(A) + (\tau_1 + \tau_2)\mathcal{L}^{-1}(B)] \tag{34}$$

What does the equation mean? We really want to know how long it takes to pull the VCO frequency to the reference. Therefore, we want to know the value of *t*, the time it takes to be within 2*p* or less of lock-in range.

The PLL can, at the beginning, have a phase error from –2*p* to +2*p*, and the loop, by accomplishing lock, then takes care of this phase error.

We can make the reverse assumption for a moment and ask ourselves, as we have done earlier, how long the loop stays in phase lock. This is called the *pull-out range*. Again, we apply signals to the input of the PLL as long as loop can follow and the phase error does not become larger than 2*p*. Once the error is larger than 2*p*, the loop jumps out of lock.

When the loop is out of lock, a beat note occurs at the output of the loop filter following the phase/frequency detector.

The tri-state phase/frequency comparator, however, works on a different principle, and the pulses generated and supplied to the charge pump do not allow the generation of an ac voltage. The output of such a phase/frequency detector is always unipolar, but relative to the value of $V_{batt}/2$, the integrator voltage can be either positive or negative. If we assume for a moment that this voltage should be the final voltage under a locked condition, we will observe that the resulting dc voltage is either more negative or more positive relative to this value, and because of this, the VCO will be "pulled in" to this final frequency rather than swept in. The swept-in technique applies only in cases of phase/frequency comparators, where this beat note is being generated. A typical case would be the exclusive-OR gate or even a sample/hold comparator. This phenomenon is rarely covered in the literature and is probably discussed in detail for the first time in the book by Roland Best [1].

Let us assume now that the VCO has been pulled in to final frequency to be within 2*p* of the

final frequency, and the time t is known. The next step is to determine the lock-in characteristic.

Lock-in Characteristic. We will now determine lock-in characteristic, and this requires the use of a different block diagram. Figure 5 shows the familiar block diagram of the PLL, and we will use the following definitions:

$$\theta_1(s) = \mathcal{L}[\Delta\delta_1(t)] \quad \text{Reference input to } \delta/\omega \text{ detector}$$
$$\theta_2(s) = \mathcal{L}[\Delta\delta_2(t)] \quad \text{Signal VCO output phase}$$
$$\theta_e(s) = \mathcal{L}[\delta_e(t)] \quad \text{Phase error at } \delta/\omega \text{ detector}$$
$$\theta_e(s) = \theta_1(s) - \frac{\theta_2(s)}{N}$$

From the block diagram, the following is apparent:

$$A(s) = \theta_e(s)K_d$$
$$B(s) = A(s)F(s)$$
$$\theta_2(s) = B(s)\frac{K_o}{s}$$

The phase error at the detector is

$$\theta_e(s) = \theta_1(s)\frac{sN}{K_oK_dF(s) + sN} \tag{35}$$

A step in phase at the input, with the worst-case error being $2p$, results in

$$\theta_1(s) = 2\pi\frac{1}{s} \tag{36}$$

We will now treat the two cases using an active or passive filter.

Active Filter. The transfer characteristic of the active filter is

$$F(s) = \frac{1 + s\tau_2}{s\tau_1} \tag{37}$$

This results in the formula for the phase error at the detector,

$$\theta_e(s) = 2\pi\frac{s}{s^2 + (sK_oK_d\tau_2/\tau_1)/N + (K_oK_d/\tau_1)/N} \tag{38}$$

The polynomial coefficients for the denominator are

$$a_2 = 1$$
$$a_1 = (K_o K_d \tau_2/\tau_1)/N$$
$$a_0 = (K_o K_d/\tau_1)/N$$

and we have to find the roots W_1 and W_2. Expressed in the form of a polynomial coefficient, the phase error is

$$\theta_e(s) = 2\pi \frac{s}{(s + W_1)(s + W_2)} \tag{39}$$

After the Laplace transformation has been performed, the result can be written in the form

$$\delta_e(t) = 2\pi \frac{W_1 e^{-W_1 t} - W_2 e^{-W_2 t}}{W_1 - W_2} \tag{40}$$

with

$$\lim_{t \to 0} \delta_e(t) = 2\pi$$

and

$$\lim_{t \to \infty} \delta_e(t) = 0$$

The same can be done using a passive filter.

Passive Filter. The transfer function of the passive filter is

$$F(s) = \frac{1 + s\tau_2}{1 + s(\tau_1 + \tau_2)} \tag{41}$$

If we apply the same phase step of $2p$ as before, the resulting phase error is

$$\theta_e(s) = 2\pi \frac{[1/(\tau_1 + \tau_2)] + s}{s^2 + s \dfrac{N + K_o K_d \tau_2}{N(\tau_1 + \tau_2)} + \dfrac{K_o K_d}{N(\tau_1 + \tau_2)}} \tag{42}$$

Again, we have to find the polynomial coefficients, which are

$$a_2 = 1$$

$$a_1 = \frac{N + K_o K_d \tau_2}{N(\tau_1 + \tau_2)}$$

$$a_0 = \frac{K_o K_d}{N(\tau_1 + \tau_2)}$$

and finally find the roots for W_1 and W_2. This can be written in the form

$$\theta_e(s) = 2\pi\left[\frac{1}{\tau_1 + \tau_2}\frac{1}{(s + W_1)(s + W_2)} + \frac{s}{(s + W_1)(s + W_2)}\right] \tag{43}$$

Now we perform the Laplace transformation and obtain our result:

$$\delta_e(t) = 2\pi\left(\frac{1}{\tau_1 + \tau_2}\frac{e^{-W_1 t} - e^{-W_2 t}}{W_2 - W_1} + \frac{W_1 e^{-W_1 t} - W_2 e^{-W_2 t}}{W_1 - W_2}\right) \tag{44}$$

with

$$\lim_{t \to 0} \delta_e(t) = 2\pi$$

with

$$\lim_{t \to \infty} \delta_e(t) = 0$$

When analyzing the frequency response for the various types and orders of PLLs, the phase margin played an important role. For the transient time, the Type 2, second-order loop can be represented with a damping factor or, for higher orders, with the phase margin. Figure 6 shows the normalized output response for a damping factor of 0.1 and 0.47. The ideal Butterworth response would be a damping factor of 0.7, which correlates with a phase margin of 45°.

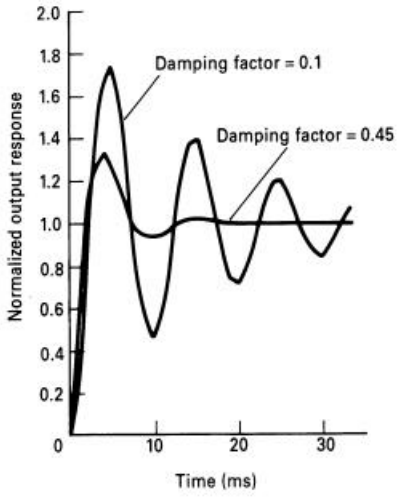


Figure 6--Normalized output response of a Type 2, second-order loop with a damping factor of 0.1 and 0.05 for $\Omega_n = 0.631$.

1-3 Loop Gain/Transient Response Examples

Given the simple filter shown in Figure 7 and the parameters as listed, the Bode plot is shown in Figure 8. This approach can also be translated from a Type 1 into a Type 2 filter as shown in Figure 9 and its frequency response as shown in Figure 10. The lock-in function for this Type 2, second-order loop with an ideal damping factor of 0.707 (Butterworth response) is shown in Figure 11. Figure 12 shows an actual settling-time measurement. Any deviation from ideal damping, as we'll soon see, results in ringing (in an underdamped system) or, in an overdamped system, the voltage will crawl to its final value. This system can be increased in its order by selecting a Type 2, third-order loop using the filter shown in Figure 13. For an ideal synthesis of the values, the Bode diagram looks as shown in Figure 14 and its resulting response is given in Figure 15.

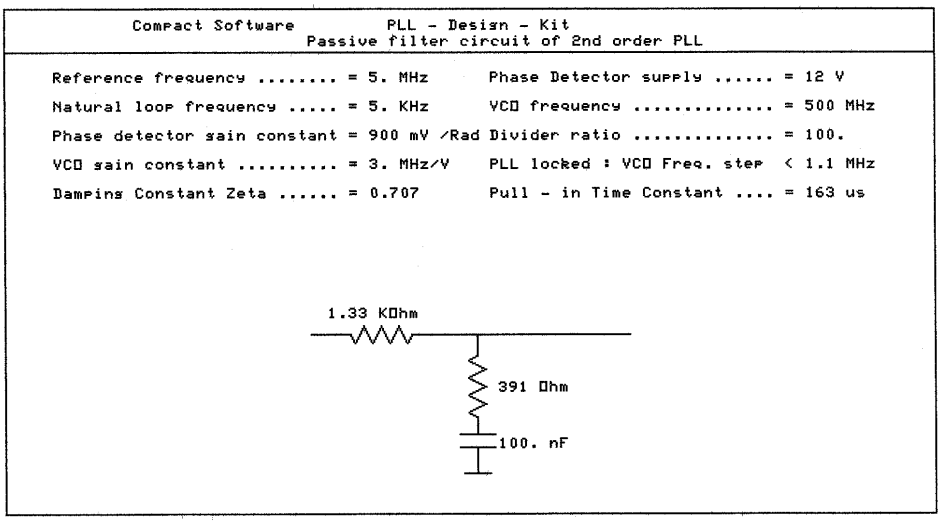


Figure 7--Loop filter for a Type 1, second-order synthesizer

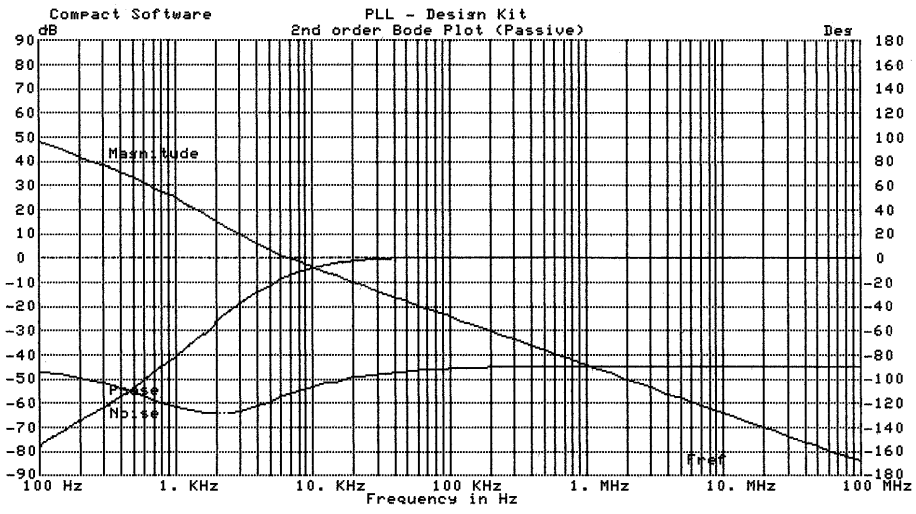


Figure 8--Type 1, second-order loop response.

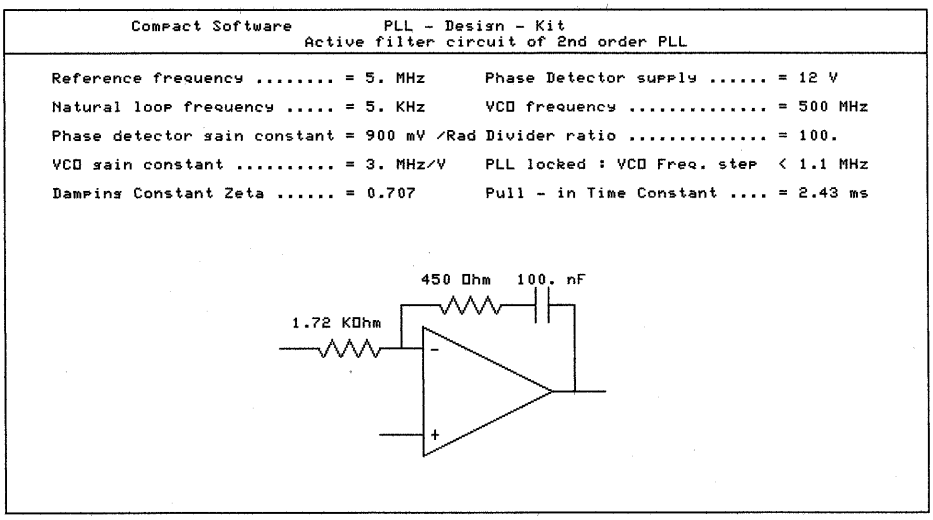


Figure 9--Loop filter for a Type 2, second-order synthesizer.

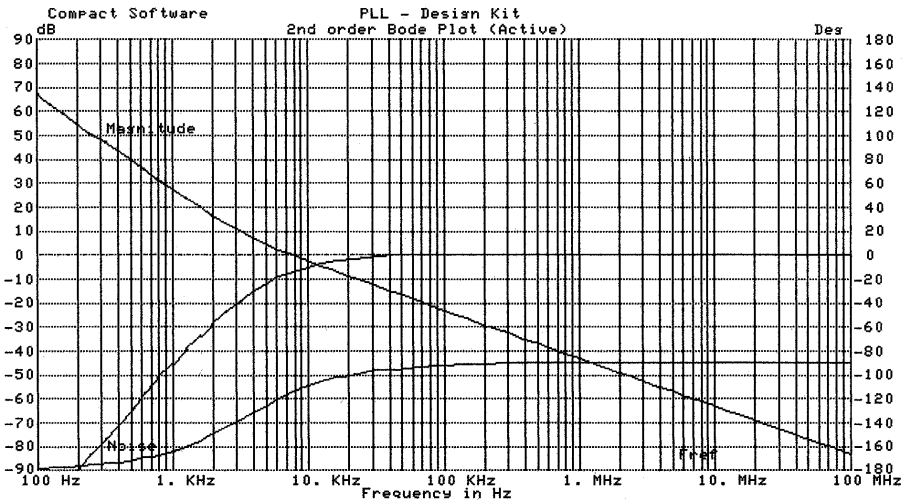


Figure 10--Response of the Type 2, second-order loop.

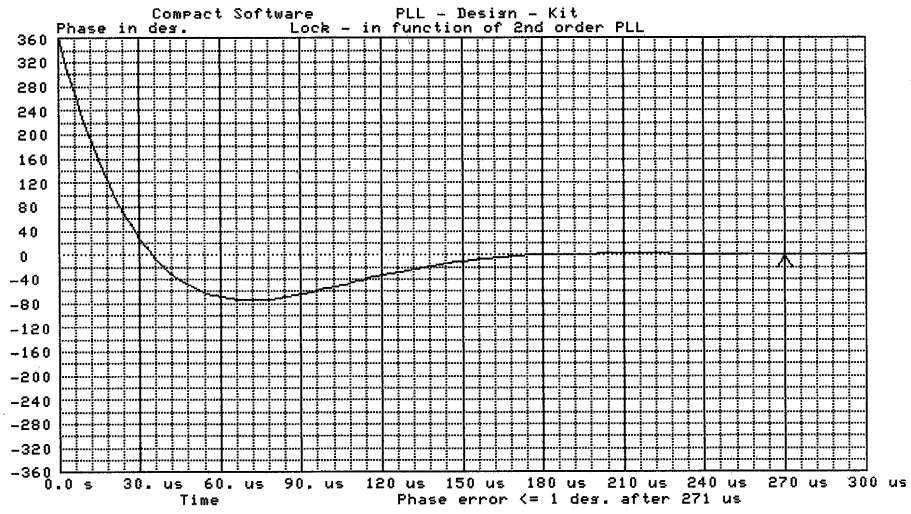


Figure 11--Lock-in function of the Type 2, second-order PLL. It indicates a lock time of 271 μs and an ideal response.

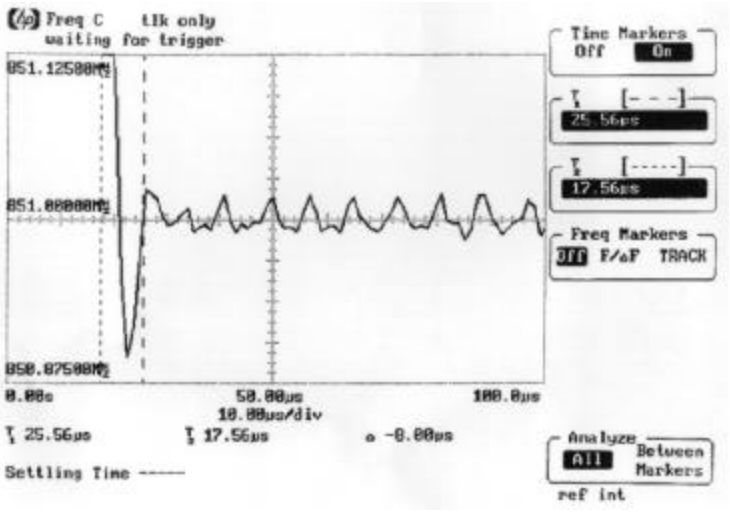


Figure 12--Example of settling-time measurement.

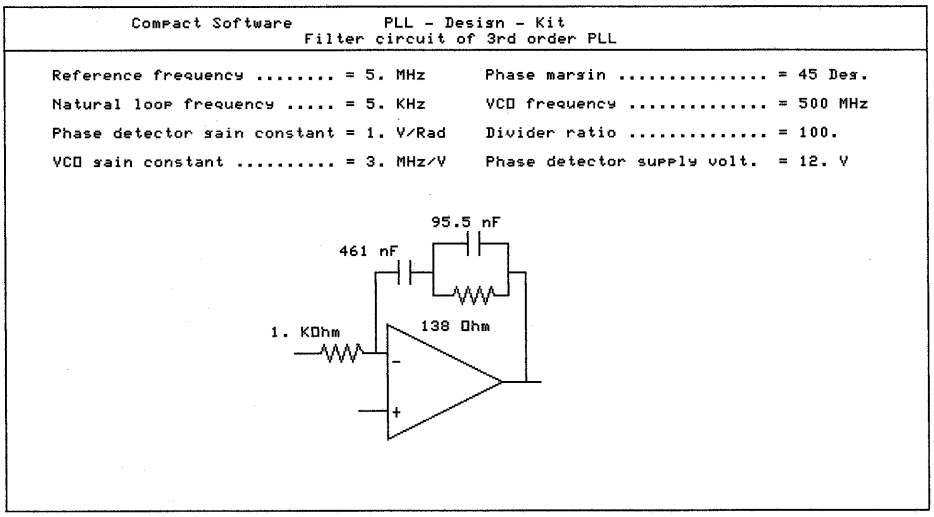


Figure 13--Loop filter for a Type 2, third-order synthesizer.

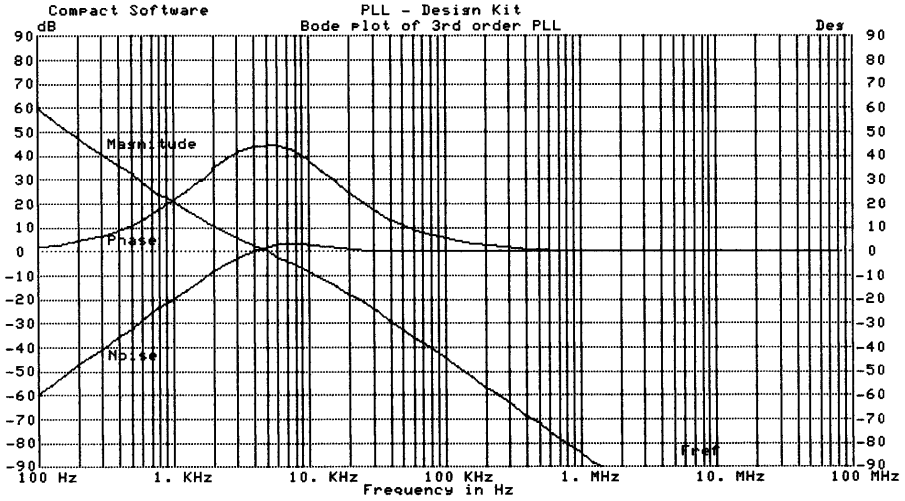


Figure 14--Open-loop Bode diagram for the Type 2, third-order loop. It fulfills the requirement of 45° phase margin at the 0-dB crossover point, and corrects the slope down to –10 dB gain.

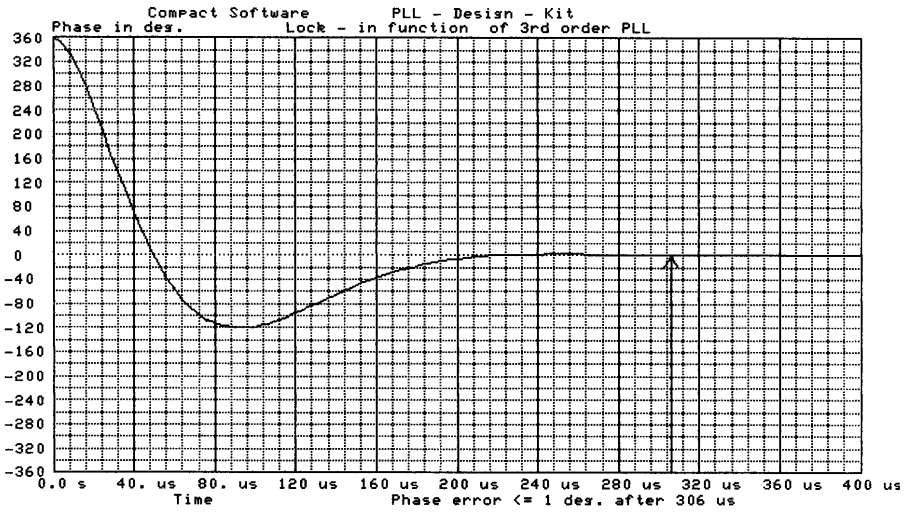


Figure 15--Lock-in function of the Type 2, third-order loop for an ideal 45° phase margin.

The order can be increased by adding an additional low-pass filter after the standard loop filter. The resulting system is called a Type 2, fifth-order loop. Figure 16 shows the Bode diagram or open-loop diagram, and Figure 17 shows the locking function. By using a very wide loop bandwidth, this can be used to clean up microwave oscillators with inherent comparatively poor phase noise. This clean-up, which will be described in more detail in Section 3, has a dramatic influence on the performance.

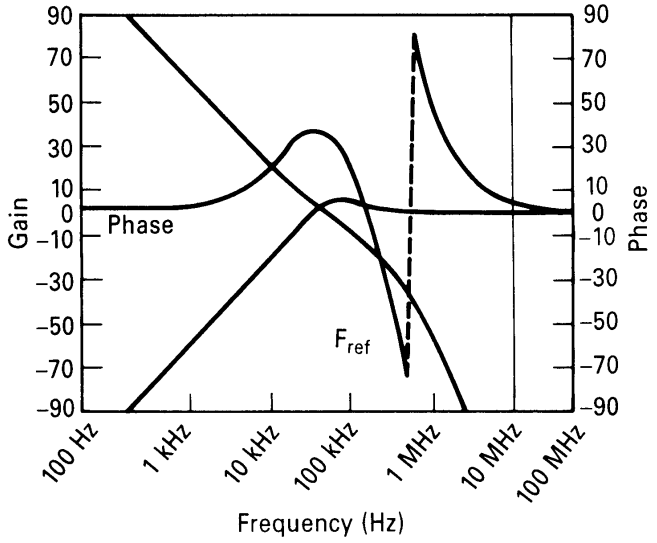


Figure 16--Bode plot of the fifth-order PLL system for a microwave synthesizer. The theoretical reference suppression is better than 90 dB.

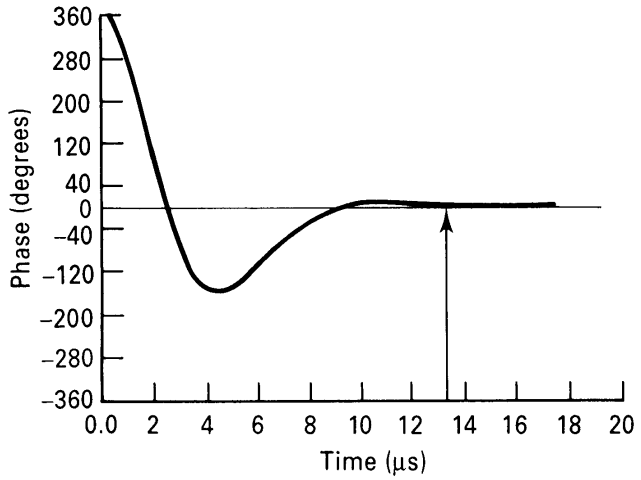


Figure 17--Lock-in function of the fifth-order PLL. Note that the phase lock time is approximately 13.3 ms.

By deviating from the ideal 45° to a phase margin of 33°, one obtains the already-mentioned ringing, as is evident from Figure 18. The time to settle has grown from 13.3 ms to 62 ms.

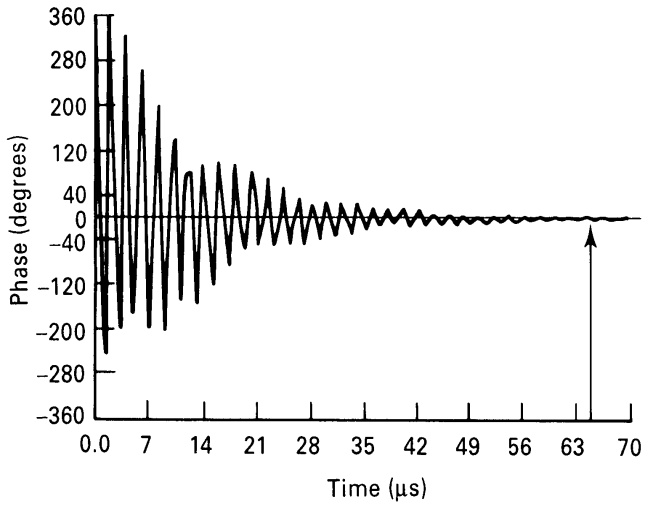


Figure 18--Lock-in function of the fifth-order PLL. Note that the phase margin has been reduced from the ideal 45°. This results in a much longer settling time of 62 ms.

To more fully illustrate the effects of nonideal phase margin, Figures 19, 20, 21, and 22 show the lock-in function of a different Type 2, fifth-order loop configured for phase margins of 25°, 35°, 45°, and 55°, respectively.

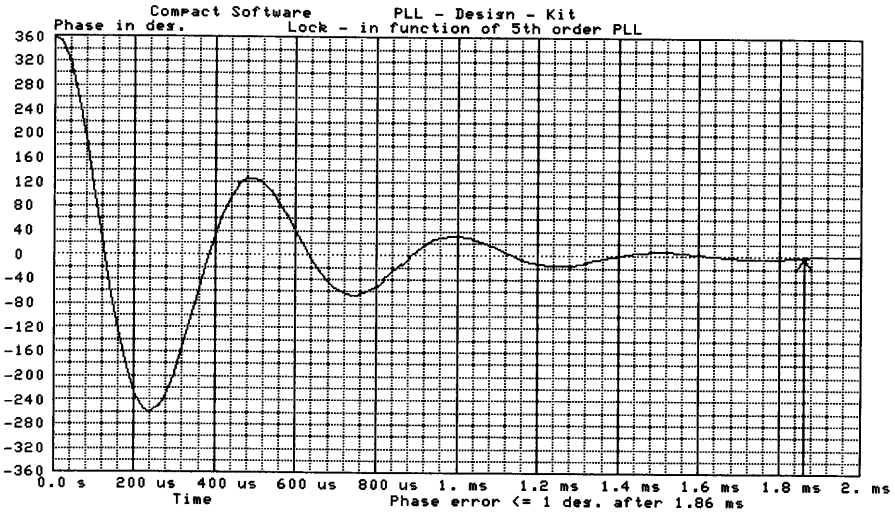


Figure 19--Lock-in function of another Type 2, fifth-order loop with a 25° phase margin. Noticeable ringing occurs, lengthening the lock-in time to 1.86 ms.

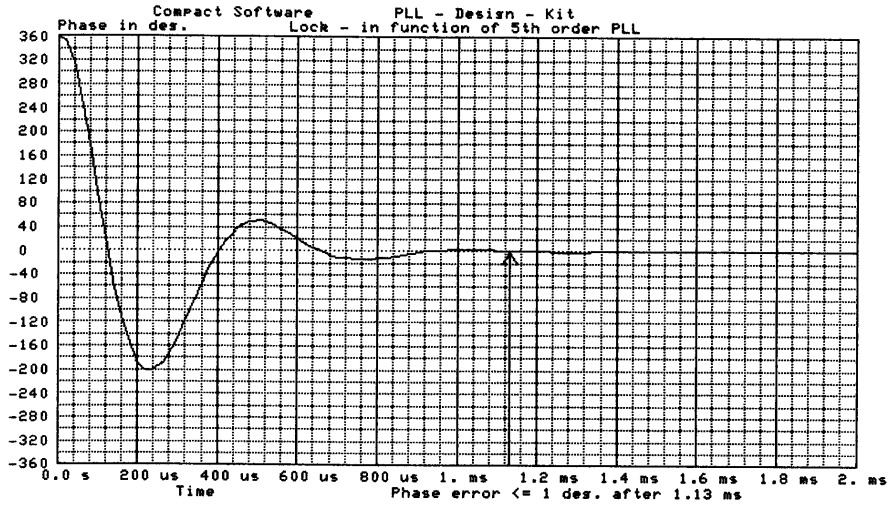


Figure 20--Lock-in function of the Type 2, fifth-order loop with a 35° phase margin. Ringing still occurs, but the lock-in time has decreased to 1.13 ms.

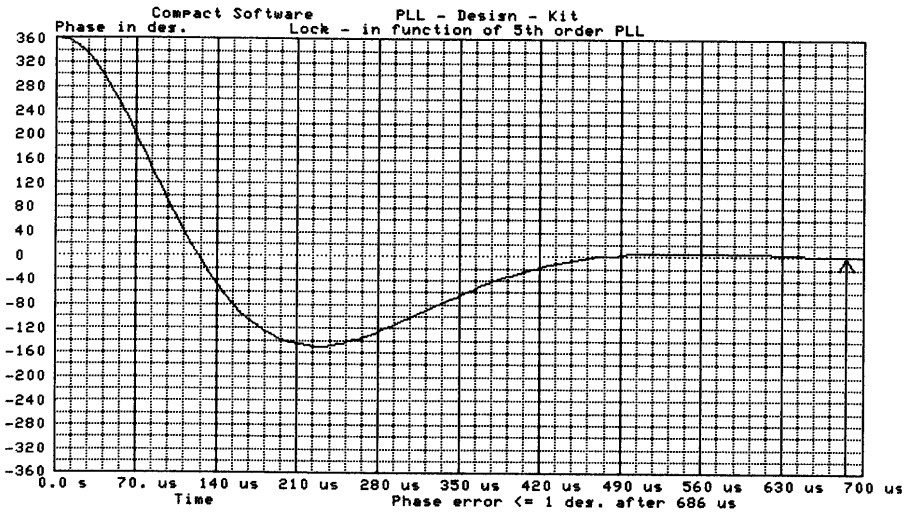


Figure 21--Lock-in function of the Type 2, third-order loop with an ideal 45° phase margin. The lock-in time is 686 *m*s.

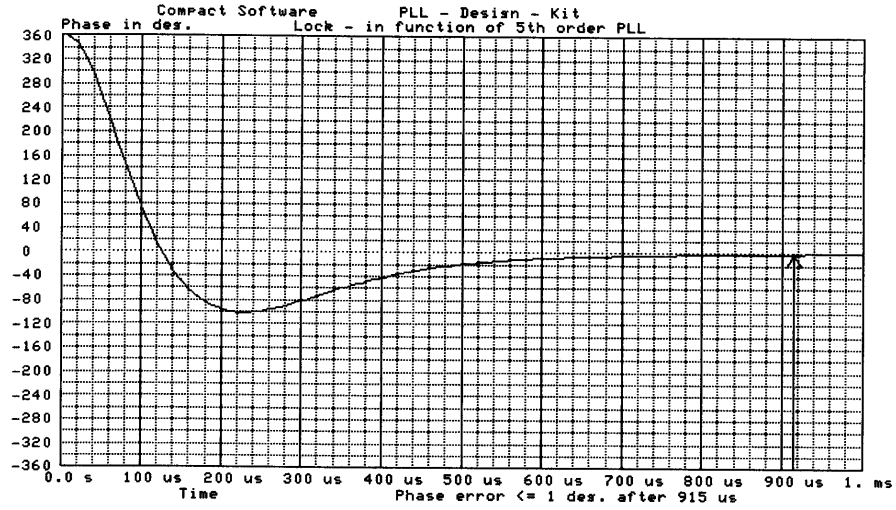


Figure 22--Lock-in function of the Type 2, fifth-order loop, for a 55° phase margin. The lock-in time has increased to 915 *m*s.

I have already mentioned that the loop should avoid "ears" (Figure 2) with poorly designed loop filters. Another interesting phenomenon (which we'll hear more about in Section 3) is the trade-off between loop bandwidth and phase noise. In Figure 23 the loop bandwidth has been made too wide, resulting in a degradation of the phase noise but provides faster settling time. By reducing the loop bandwidth from about 1 kHz to 300 Hz, only a very slight overshoot remains, improving the phase noise significantly. This is shown in Figure 24.

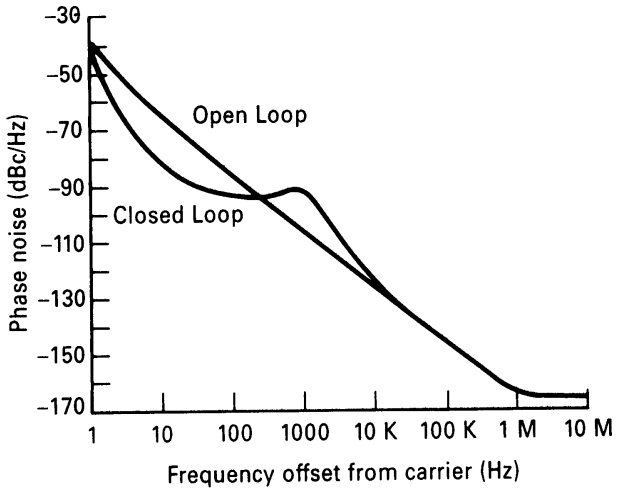


Figure 23--Comparison between open- and closed-loop noise prediction. Note the overshoot of around 1 kHz off the carrier.

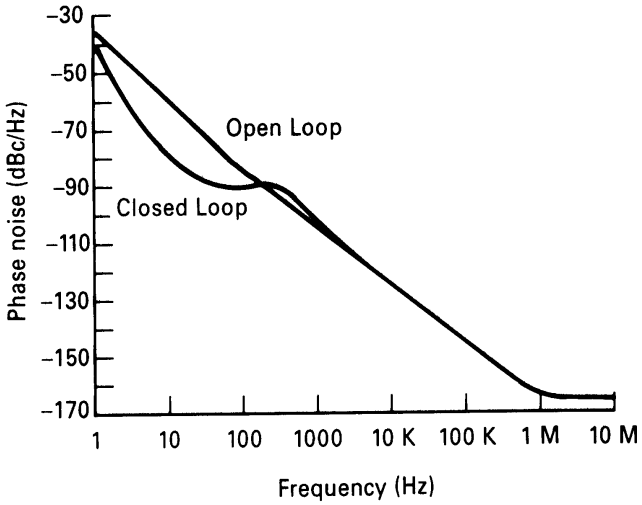


Figure 24--Comparison between open- and closed-loop noise prediction. Note the overshoot at around 300 Hz off the carrier.

1-4 Practical Circuits

Figure 25 shows a passive filter which is used for a National LMX synthesizer chip. This chip has a charge-pump output, which explains the need for the first capacitor.

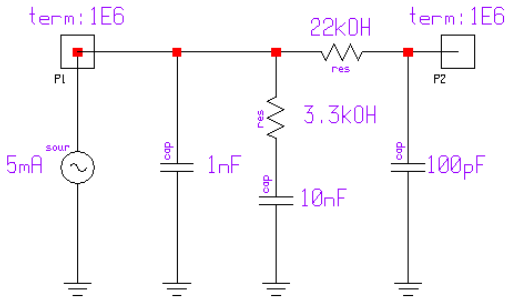


Figure 25--Type 1 high-order loop filter used for passive filter evaluation. The 1-nF capacitor is used for spike suppression as explained in the text. The filter consists of a lag portion and an additional low pass section.

Figure 26 shows an active integrator operating at a reference frequency of several megahertz. The notch filter at the output reduces the reference frequency considerably. The notch is about 4.5 MHz.

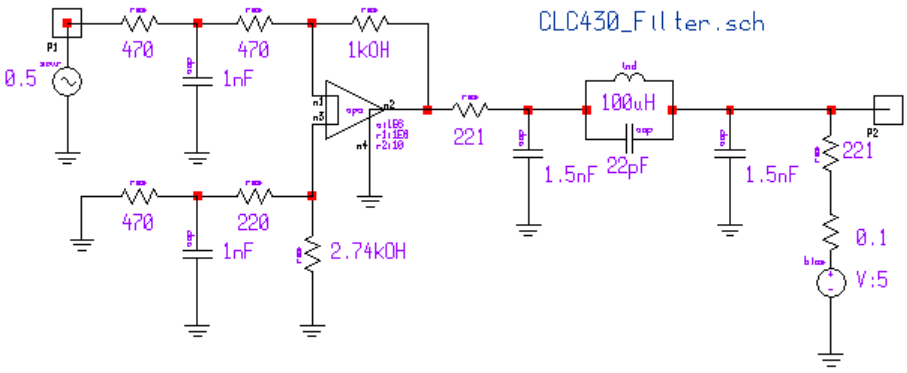


Figure 26--A Type 2 high-order filter with a notch to suppress the discrete reference spurs.

Figure 27 shows the combination of a phase/frequency discriminator and a higher-order loop filter as used in more complicated systems, such as fractional-division synthesizers.

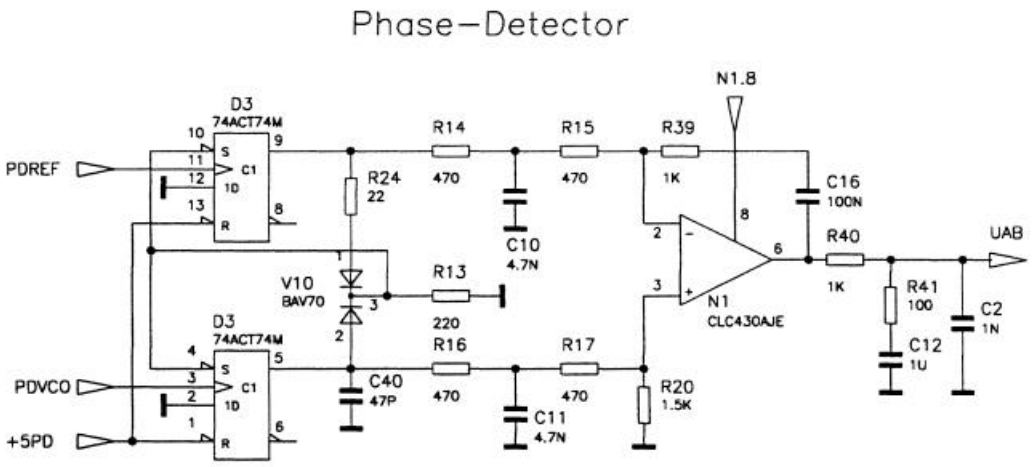


Figure 27--Phase/frequency discriminator including an active loop filter capable of operating up to 100 MHz.

Figure 28 shows a custom-built phase detector with a noise floor of better than –168 dBc/Hz.

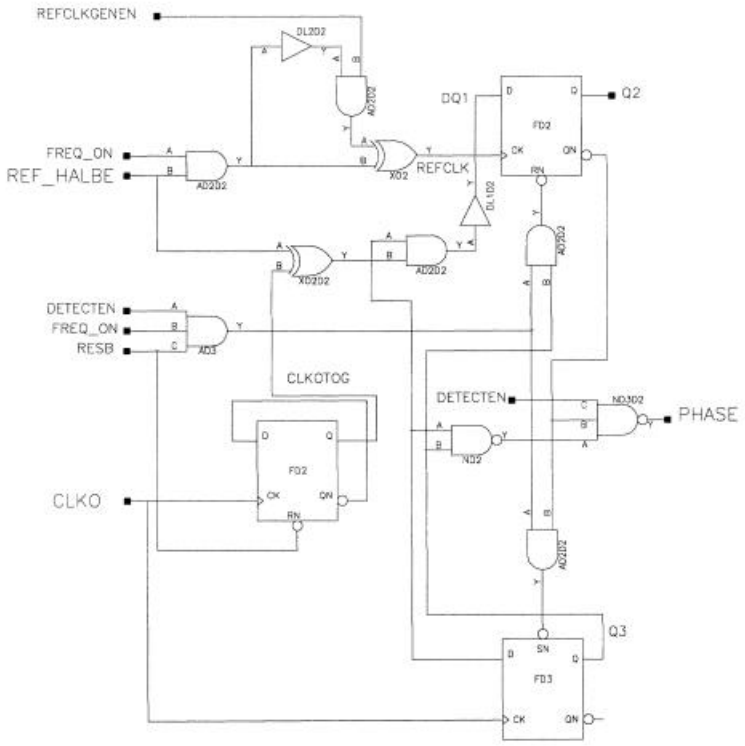


Figure 28--Custom-built phase detector with a noise floor of better than –168 dBc/Hz. This phase detector shows extremely low phase jitter.

2 FRACTIONAL-DIVISION SYNTHESIZERS

2-1 Introduction

In conventional synthesizers, the minimum step size is equal to the reference frequency. In order to get a finer resolution, we can either play games at the reference as outlined in Figure 1, or we can use fractional division. The principle of the fractional-*N*-division synthesizer has been around for a while. In the past, implementation of this has been done in an analog system. The above mentioned single loop uses a frequency divider where the division ratio is an integer value between 1 and some very large number, hopefully not as high as 50,000. It would be ideal to be able to build a synthesizer with the 1.25 MHz reference or 50 MHz reference and yet obtain the desired step size resolution such as 25 kHz. This would lead to a much smaller division ratio and better phase noise performance.

An alternative would be for N to take on fractional values. The output frequency could then be changed in fractional increments of the reference frequency. Although a digital divider cannot provide a fractional division ratio, ways can be found to accomplish the same task effectively. The most frequently used method is to divide the output frequency by $N + 1$ every M cycles and to divide by N the rest of the time. The effective division ratio is then $N + \frac{1}{M}$, and the average output frequency is given by

$$f_0 = \left(N + \frac{1}{M} \right) f_r \tag{45}$$

This expression shows that f_0 can be varied in fractional increments of the reference frequency

by varying *M*. The technique is equivalent to constructing a fractional divider, but the fractional part of the division is actually implemented using a phase accumulator. The phase accumulator approach is illustrated by the following example. This method can be expanded to frequencies much higher than 6 GHz using the appropriate synchronous dividers.

Example: considering the problem of generating 899.8 MHz using a fractional-*N* loop with a 50-MHz reference frequency, 899.8 MHz = 50 MHz $\left(N+\frac{K}{F}\right)$; the integral part of the division *N* has to be set to 17 and the fractional part $\frac{K}{F}$ needs to be $\frac{996}{1000}$; (the fractional part $\frac{K}{F}$ is not a integer) and the VCO output has to be divided by 996 × every 1,000 cycles. This can easily be implemented by adding the number 0.996 to the contents of an accumulator every cycle. Every time the accumulator overflows, the divider divides by 18 rather than by 17. Only the fractional value of the addition is retained in the phase accumulator. If we move to the lower band or try to generate 850.2 MHz, *N* remains 17 and $\frac{K}{F}$ becomes $\frac{4}{1000}$. This method of using fractional division was first introduced by using analog implementation and noise cancellation, but today it is implemented as a totally digital approach. The necessary resolution is obtained from the dual-modulus prescaling, which allows for a well-established method for achieving a high-performance frequency synthesizer operating at UHF and higher frequencies. Dual-modulus prescaling avoids the loss of resolution in a system compared to a simple prescaler; it allows a VCO step equal to the value of the reference frequency to be obtained. This method needs an additional counter and the dual-modulus prescaler then divides one or two values depending upon the state of its control. The only drawback of prescalers is the minimum division ratio of the prescaler for approximately N^2. The dual modulus divider is the key to implementing the fractional-*N* synthesizer principle. Although the fractional-*N* technique appears to have a good potential of solving the resolution limitation, it is not free of having its own complications. Typically, an overflow from the phase accumulator, which is the adder with the output feedback to the input after being latched, is used to change the instantaneous division ratio. Each overflow produces a jitter at the output frequency, caused by the fractional division, and is limited to the fractional portion of the desired division ratio.

In our case, we had chosen a step size of 200 kHz, and yet the discrete side bands vary from 200 kHz for $\frac{K}{F} = \frac{4}{1000}$ to 49.8 MHz for $\frac{K}{F} = \frac{996}{1000}$. It will become the task of the loop filter to remove those discrete spurious. While in the past the removal of the discrete spurs has been accomplished by using analog techniques, various digital methods are now available. The microprocessor has to solve the following equation:

$$N^* = \left(N + \frac{K}{F}\right) = \left[N(F-K) + (N+1)K\right] \tag{46}$$

Example

For $F_0 = 850.2$ MHz, we obtain:

$$N^* = \frac{850.2 \text{ MHz}}{50 \text{ MHz}} = 17.004$$

Following the formula above:

$$N^* = \left(N + \frac{K}{F} \right) = \frac{\left[17(1000 - 4) + (17 + 1) \times 4 \right]}{1000}$$

$$= \frac{\left[16932 + 72 \right]}{1000} = 17.004$$

$$F_{out} = 50 \text{ MHz} \times \frac{\left[16932 + 72 \right]}{1000}$$

$$= 846.6 \text{ MHz} + 3.6 \text{ MHz}$$

$$= 850.2 \text{ MHz}$$

By increasing the number of accumulators, frequency resolution much below a step size of 1 Hz is possible with the same switching speed.

2-2 Spur-Suppression Techniques

While several methods have been proposed in the literature (see patents in references 2-7), the method of reducing the noise by using a $\Sigma\Delta$ modulator has shown to be most promising. The concept is to get rid of the low-frequency phase error by rapidly switching the division ratio to eliminate the gradual phase error at the discriminatory input. By changing the division ratio rapidly between different values, the phase errors occur in both polarities, positive as well as negative, and at an accelerated rate that explains the phenomenon of high-frequency noise push-up. This noise, which is converted to a voltage by the phase/frequency discriminator and loop filter, is filtered out by the low-pass filter. The main problem associated with this noise shaping technique is that the noise power rises rapidly with frequency. Figure 29 shows noise contributions with such a $\Sigma\Delta$ modulator in place.

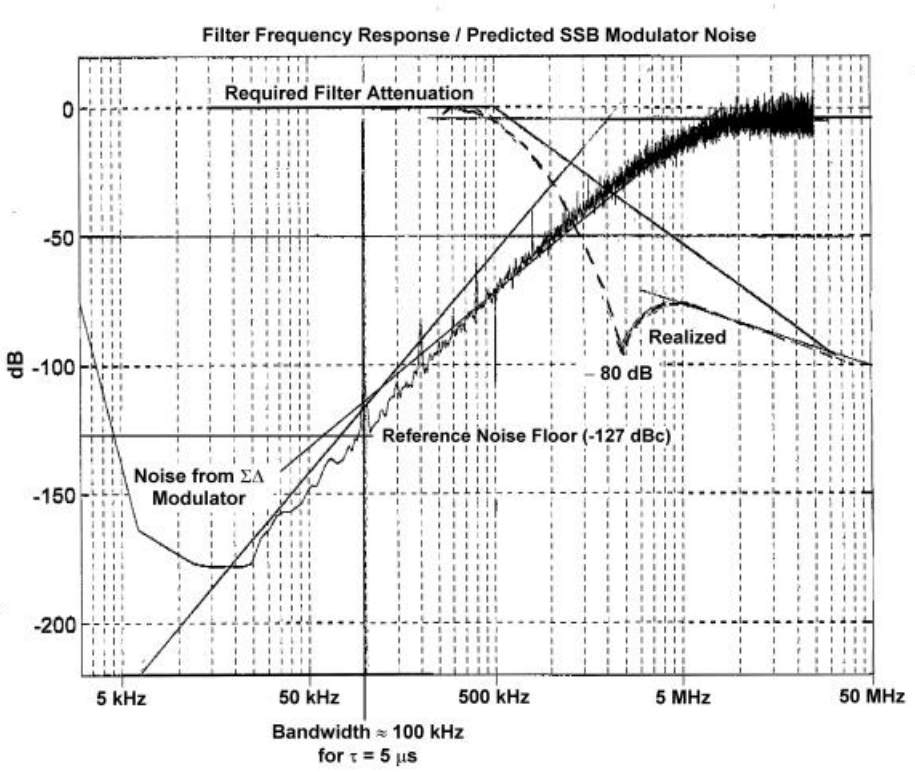


Figure 29--The filter frequency response/phase noise analysis graph shows the required attenuation for the reference frequency of 50 MHz and the noise generated by the ΣΔ converter (three steps) as a function of the offset frequency. It becomes apparent that the ΣΔ converter noise dominates above 80 kHz unless attenuated.

On the other hand, we can now, for the first time, build a single-loop synthesizer with switching times as fast as 6 *m*s and very little phase-noise deterioration inside the loop bandwidth, as seen in Figure 29. Since this system maintains the good phase noise of the ceramic-resonator-based oscillator, the resulting performance is significantly better than the phase noise expected from high-end signal generators. However, this method does not allow us to increase the loop bandwidth beyond the 100-kHz limit, where the noise contribution of the ΣΔ modulator takes over.

Table 2--Comparison of Spur-Suppression Methods

Technique	Feature	Problem
DAC Phase Estimation	Cancel Spur by DAC	Analog Mismatch
Pulse Generation	Insert Pulses	Interpolation Jitter
Phase Interpolation	Inherent Fractional Divider	Interpolation Jitter
Random Jittering	Randomize Divider	Frequency Jitter
ΣΔ Modulation	Modulate Division Ratio	Quantization Noise

Table 2 shows some of the modern spur suppression methods. These three-stage ΣΔ methods with larger accumulators have the most potential [2-7].

The power spectral response of the phase noise for the three-stage ΣΔ modulator is calculated from:

$$L(f) = \frac{(2p)^2}{12 \cdot f_{ref}} \cdot \left[2\sin\left(\frac{p \quad f}{f_{ref}} \right) \right]^{2(n-1)} \text{ rad}^2/\text{Hz} \tag{47}$$

where n is the number of the stage of the cascaded sigma-delta modulator [8]. Equation (47) shows that the phase noise resulting from the fractional controller is attenuated to negligible levels close to the center frequency, and further from the center frequency, the phase noise is increased rapidly and must be filtered out prior to the tuning input of the VCO to prevent unacceptable degradation of spectral purity. A loop filter must be used to filter the noise in the PLL loop. Figure 29 showed the plot of the phase noise versus the offset frequency from the center frequency. A fractional-N synthesizer with a three-stage ΣΔ modulator as shown in Figure 30 has been built. The synthesizer consists of a phase/frequency detector, an active low-pass filter (LPF), a voltage-controlled oscillator (VCO), a dual-modulus prescaler, a three-stage ΣΔ modulator, and a buffer.

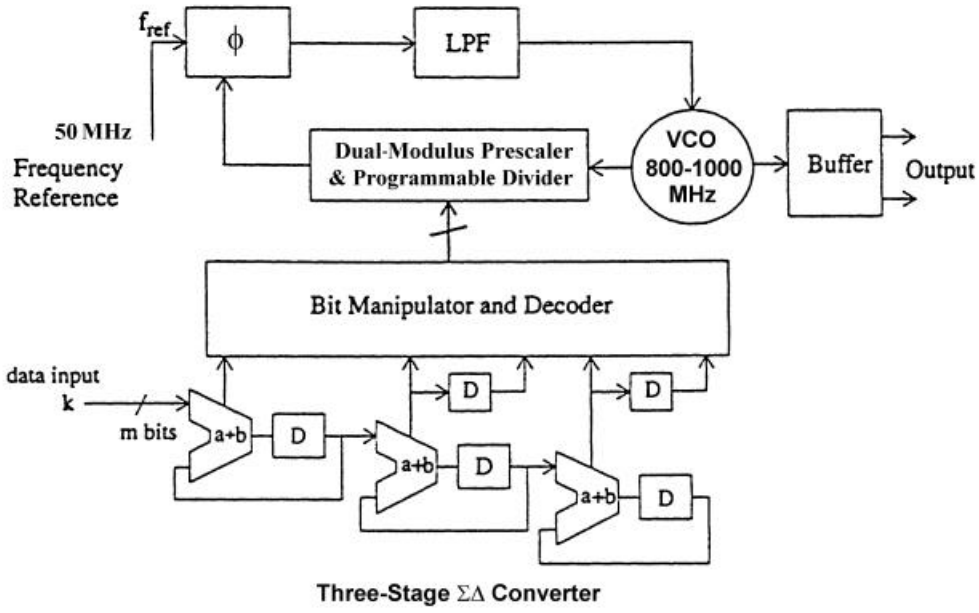


Figure 30--A block diagram of the fractional-*N*-division synthesizer built using a custom IC. Designed to operate with input frequencies up to 100 MHz, it uses the phase/frequency discriminator shown in Figure 27.

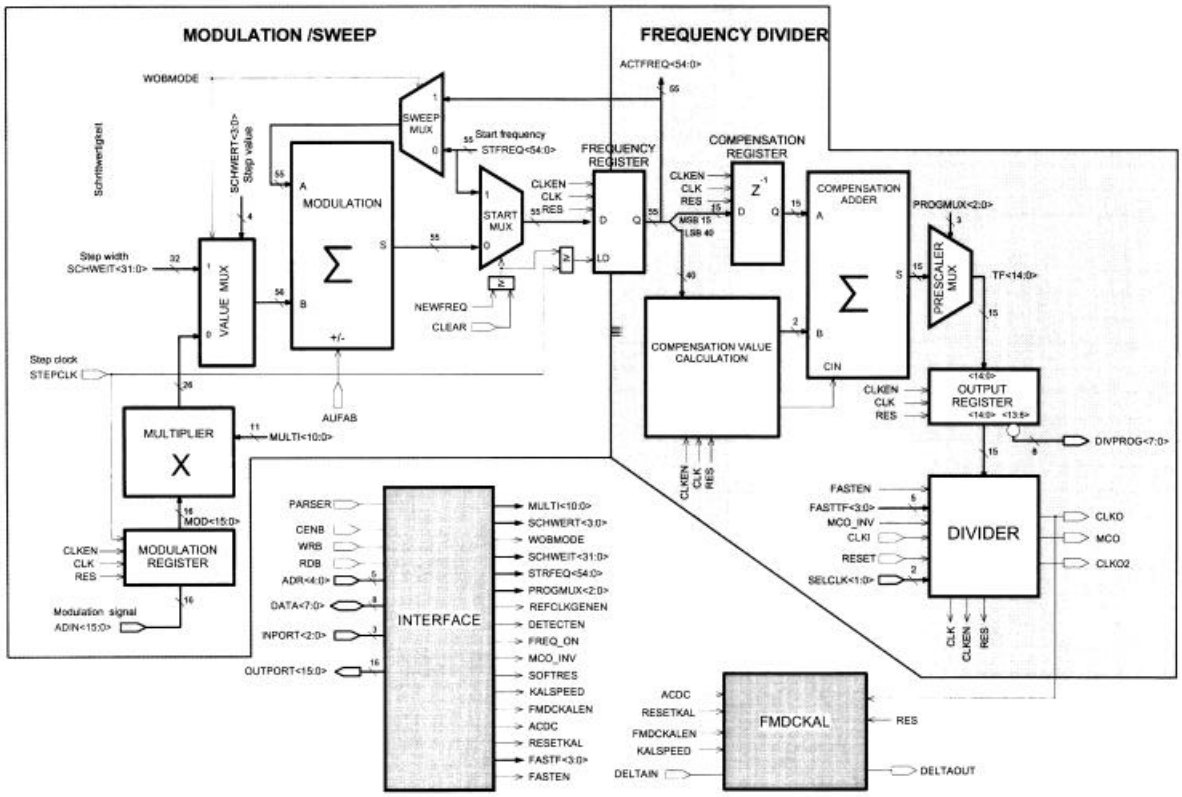


Figure 31--Detailed block diagram of the inner workings of the fractional-*N*-division synthesizer chip.

After designing, building, and predicting the phase noise performance of this synthesizer, it becomes clear that the phase noise measurement for such a system would become tricky. The standard measurement techniques with a reference synthesizer would not provide enough resolution because there are no synthesized signal generators on the market sufficiently good enough to measure its phase noise. Therefore, we had to build a comb generator that would take the output of the oscillator and multiply this up 10 to 20 times.

Passive phase-noise measurement systems, based on delay lines, are not selective, and the comb generator confuses them; however, the Rohde & Schwarz FSEM spectrum analyzer with the K-4 option has sufficient resolution to be used for phase-noise measurements. All of the Rohde & Schwarz FSE series spectrum analyzers use a somewhat more discrete fractional-division synthesizer with a 100-MHz reference. Based on the multiplication factor of 10, it turns out that there is enough dynamic range in the FSEM analyzer with the K-4 option to be used for phase-noise measurement. The useful frequency range off the carrier for the system is 100 Hz to 10 MHz--perfect for this measurement.

Figure 32 shows the measured phase noise of the final frequency synthesizer.

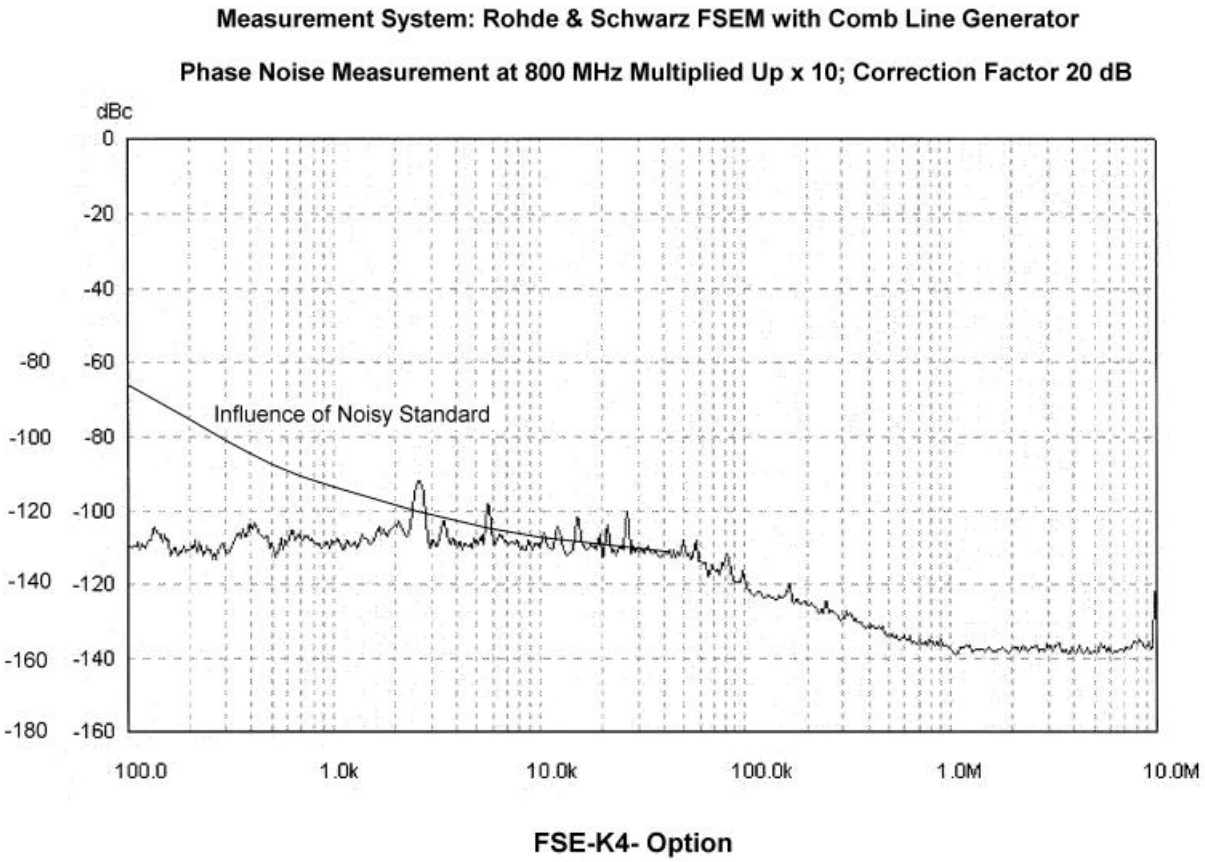


Figure 32--Measured phase noise of the fractional-*N*-division synthesizer using a custom-built, high-performance 50-MHz crystal oscillator as a reference, with the calculated degradation due to a noisy reference plotted for comparison. Both synthesizer and spectrum analyzer use the same reference.

During the measurements, it was also determined that the standard crystal oscillator we were using was not good enough. We therefore needed to develop a 50-MHz crystal oscillator with better phase noise. Upon examination of the measured phase noise shown in Figure 32, it can been seen that the oscillator used as the reference was significantly better. Otherwise, this phase noise would not have been possible. The loop filter cutoff frequency of about 100 kHz can be recognized by the roll-off in Figure 32. This fractional-*N*-division synthesizer with a high-performance VCO has a significantly better phase noise than other example systems in this frequency range. In order to demonstrate this improvement, phase-noise measurements were made on standard systems, using typical synthesizer chips. While the phase noise by itself and the synthesizer design is quite good, it is no match for this new approach, as can be seen in Figure 33 [9].

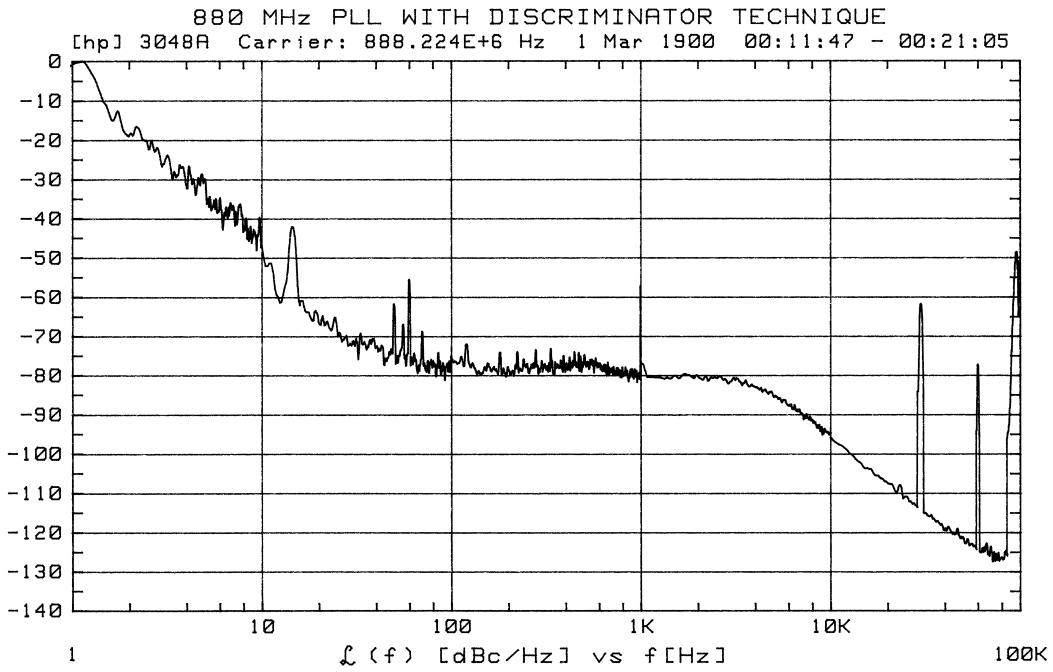


Figure 33--Measured phase noise of a 880-MHz synthesizer using a conventional synthesizer chip. Comparing this to Figure 32 shows the big improvement possible with fractional-*N*-division synthesizers.

This scheme can be extended by using an additional loop with a comb generator and translating the higher-frequency, such as microwave or millimeterwave, down to a frequency at which the fractional system can operate. Currently available ICs limit this principle to about 1 GHz because of prescaler noise. A nice application showing how to combine fractional-division synthesizers and microwave oscillators, such as YIG types, is shown in Figure 34.

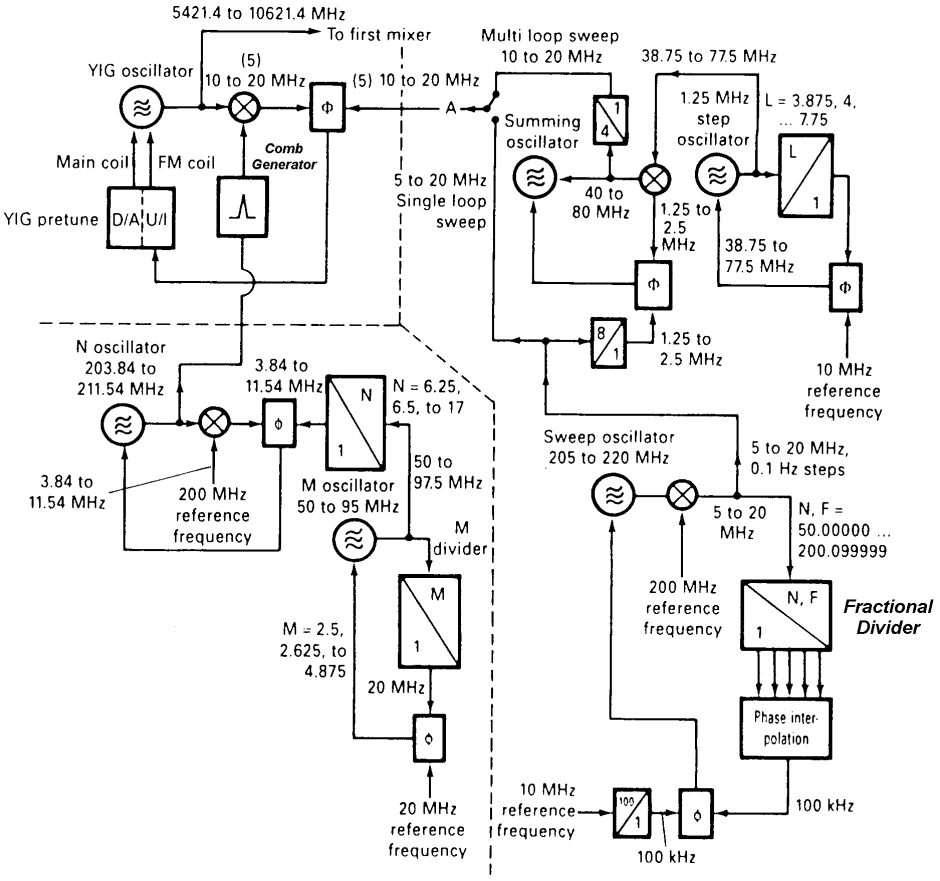


Figure 34--Interaction of the frequency-determining modules of the first local oscillator of a microwave spectrum analyzer.

3 NOISE IN SYNTHESIZERS

3-1 Phase Noise of Oscillators

All elements of a synthesizer contribute to noise. The two primary noise contributors are the reference and the VCO. Actually, the crystal oscillator or frequency standard is a high-*Q* version of the VCO. They are both oscillators, one electronically tunable over a high-percentage range and the other one tunable just enough to compensate for aging.

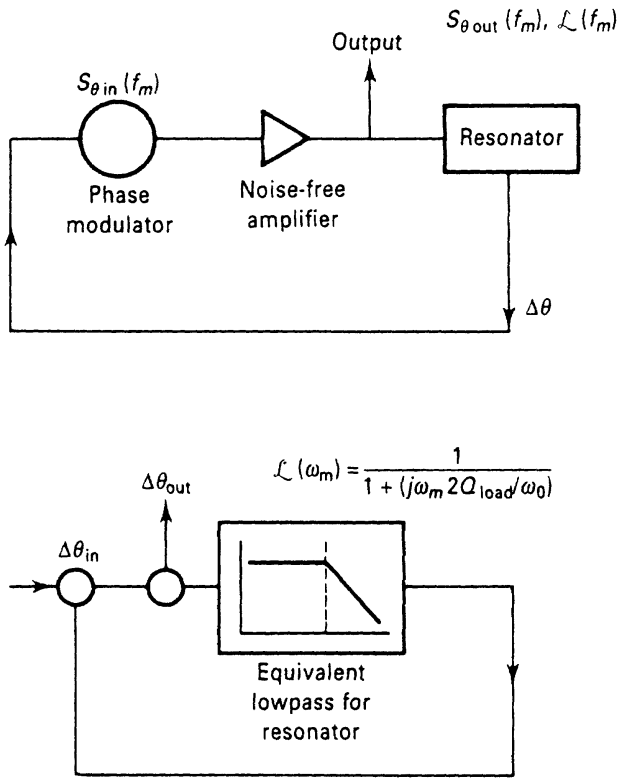


Figure 35--Equivalent feedback models of oscillator phase noise.

Leeson introduced a linear approach for the calculation of oscillator phase noise (Figure 35). His formula was extended by Scherer and Rohde. Scherer added the flicker corner frequency calculation to it and I added the VCO term. The phase noise of a VCO is determined by

$$\mathcal{L}(f_m) = 10\log\left\{\left[1+\frac{f_0^{\,2}}{(2f_mQ_{load})^2}\right]\left(1+\frac{f_c}{f_m}\right)\frac{FkT}{2P_{sav}}+\frac{2kTRK_0^{\,2}}{f_m^{\,2}}\right\} \tag{48}$$

where

$\mathcal{L}(f_m)$ = ratio of sideband power in a 1-Hz bandwidth at f_m to total power in dB
f_m = frequency offset
f_0 = center frequency
f_c = flicker frequency
Q_{load} = loaded Q of the tuned circuit
F = noise factor
$kT = 4.1 \times 10^{-21}$ at 300 K (room temperature)
P_{sav} = average power at oscillator output
R = equivalent noise resistance of tuning diode (typically 200 Ω to 10 kΩ)
K_0 = oscillator voltage gain

When adding an isolating amplifier, the noise of an *LC* oscillator is determined by

$$S_\phi(f_m) = \left[a_R F_0^4 + a_E (F_0/(2Q_L))^2\right] / f_m^3$$
$$+ \left[\left(2GFkT / P_0\right)\left(F_0/\left(2Q_L\right)\right)^2\right] / f_m^2$$
$$+ \left(2a_R Q_L F_0^3\right) / f_m^2$$
$$+ a_E / f_m + 2GFkT / P_0 \qquad (49)$$

where

G = compressed power gain of the loop amplifier
F = noise factor of the loop amplifier
k = Boltzmann's constant
T = temperature in kelvins
P_0 = carrier power level (in watts) at the output of the loop amplifier
F_0 = carrier frequency in Hz
f_m = carrier offset frequency in Hz
$Q_L(=pF_0t_g)$ = loaded Q of the resonator in the feedback loop
a_R and a_E = flicker noise constants for the resonator and loop amplifier, respectively

In order to evaluate the consequences of the above-stated linear equation, we are going to run several examples. Figure 36 shows the predicted phase noise of a crystal oscillator at 5 MHz with an operating Q of 1E6. High-end crystal oscillators typically use crystals with such a high Q. At the same time, we plot the phase noise prediction for a 4-GHz VCO with a tuning sensitivity of 10 MHz/V and operating Q of 400. This is only achievable with a loosely coupled ceramic resonator. The next logical step is to multiply the 5 MHz to 4 GHz, resulting in the second curve parallel to the crystal oscillator curve. As the caption for the figure indicates, the crossover point between the multiplied phase noise and the 4-GHz oscillator determines the best loop bandwidth.

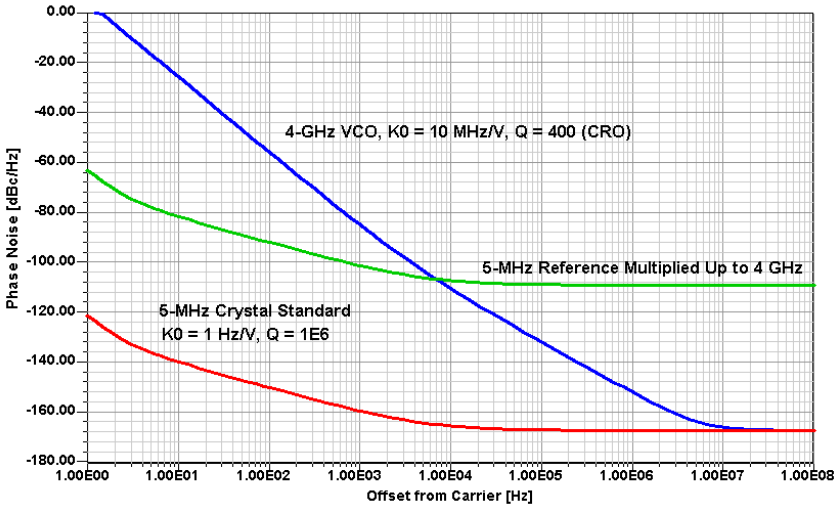


Figure 36--Predicted phase noise for a 5-MHz crystal frequency standard (top-of-the-line), 4-GHz VCO, and the effect of multiplication of the frequency standard to 4 GHz. The phase noise can be improved on the left side of the intersection and will be degraded on the right side of the intersection depending on the loop bandwidth chosen. (The ideal loop bandwidth would equal to the frequency offset at the point of intersection.) This assumes that no other components, such as the phase detector and dividers, add to the noise.

Assuming for a moment that we use just the oscillator, no tuning diode attached, and therefore consider only the first two terms in the equations above, we can evaluate the phase noise as a function of the loaded *Q* of the tuned circuit. Figure 37 shows this evaluation. The *Q* of 4000 is not realistic, but is calculated to show the theoretical limit. Again, this is *not* a VCO.

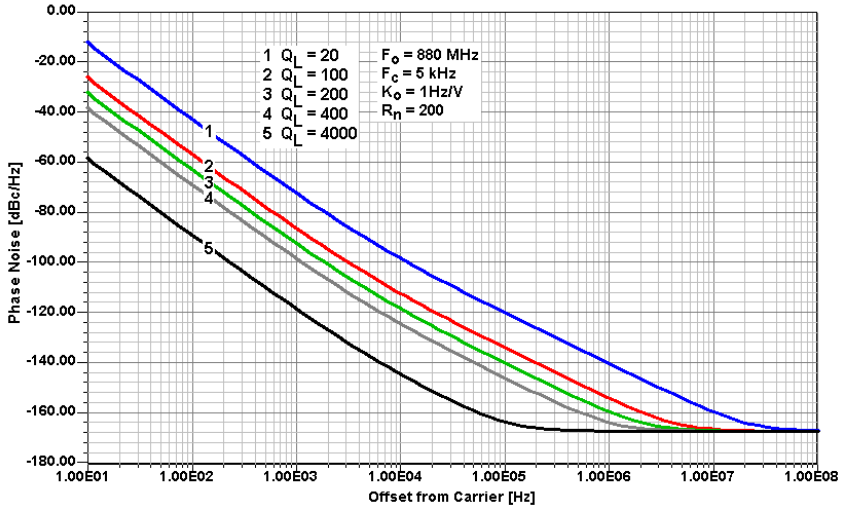


Figure 37--Predicted phase noise of an 880-MHz oscillator (*not* a VCO) as a function of the *Q*. The final *Q* (4000) can only be obtained with a large helical resonator, and is only a value given for comparison purposes; it is not practically achievable.

In the same fashion, assuming an oscillator not a VCO, we are going to inspect the result of flicker noise contribution from the transistor (Figure 38). The wide range from 50 Hz to 10 MHz covers the silicon FET, the bipolar transistor, and the GaAsFET.

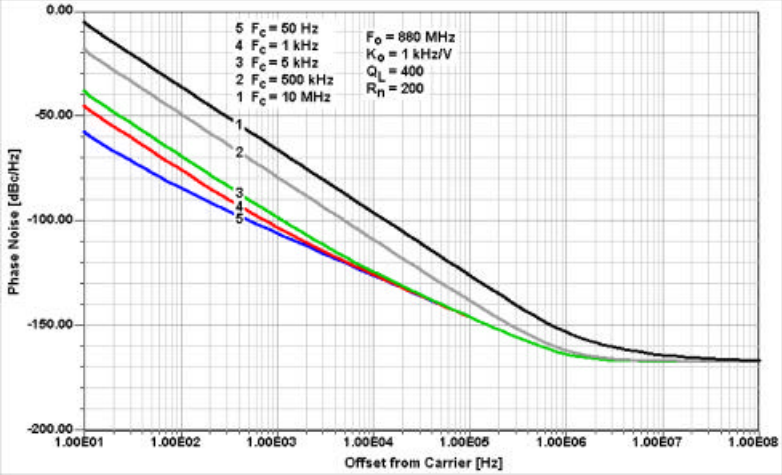


Figure 38--Predicted phase noise of an 880-MHz oscillator (*not* a VCO) with a resonator *Q* of 400, varying the flicker corner frequency from 50 Hz (silicon FET) to 10 MHz (GaAsFET).

Finally, we change the oscillator into a voltage-controlled oscillator by adding a tuning diode. Figure 39 shows the effect of the tuning diode as a function of the tuning sensitivity. In this particular case, the sensitivity above 10 MHz/V solely determines the phase noise. This fact is frequently overlooked and has nothing to do with the *Q* or leakage currents of the diode. The last term in (48) above controls this.

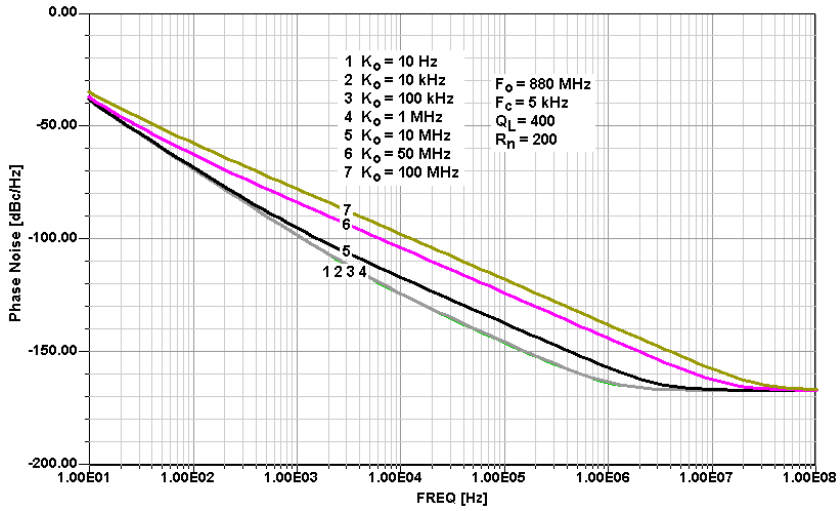


Figure 39--Predicted phase noise of an 880-MHz VCO with tuning sensitivity ranging from 10 Hz to 100 MHz/V. It *must* be noted that above a certain sensitivity--in this case, 10 MHz/V--the phase noise is determined only by the circuit's tuning diode(s) and is no longer a function of the resonator and diode *Q*.

The actual noise in the transistor therefore is modulated on an ideal carrier, referred to as IF in Figure 40. All the various noise sources are collected and superimposed on an ideal, noise-free carrier. This complex mechanism, which goes beyond the linear noise equation, is handled by a nonlinear analysis process incorporated in harmonic-balance simulators, such as the Serenade product by Ansoft, or its equivalent by Hewlett-Packard or others.

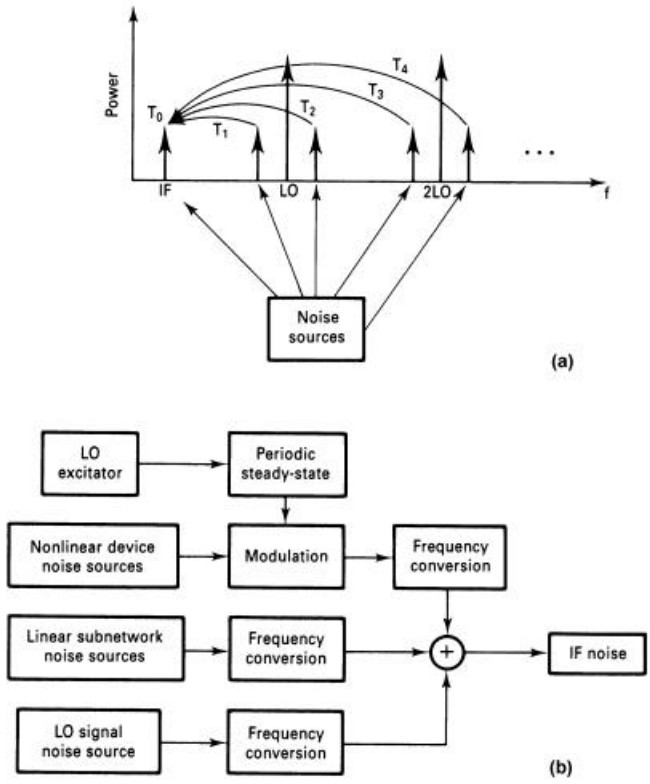


Figure 40--Summary of (*a*) noise sources mixed to the IF, and (*b*) IF noise contributions.

Oscillators are also described in the time domain. Figure 41 shows the characterization of the noise, both in the time and frequency domains, and its contributors.

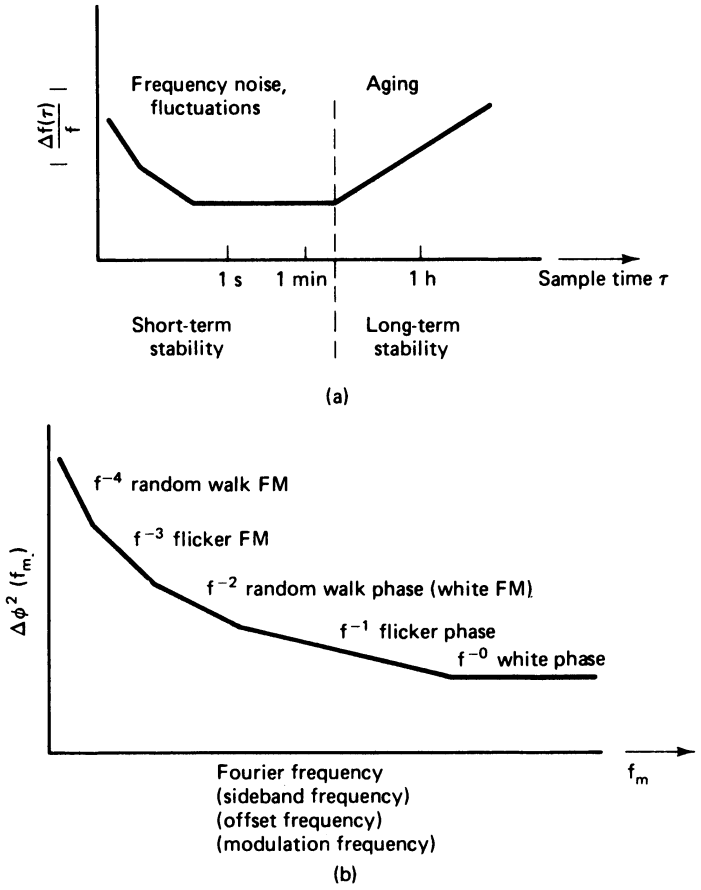


Figure 41--Characterization of a noise sideband and its contributions in the (*a*) time and (*b*) frequency domains.

The resulting phase noise is largely influenced by the operating *Q*. This was already pointed out above. Figure 42 shows the relationship between *Q* and phase noise for two extreme cases.

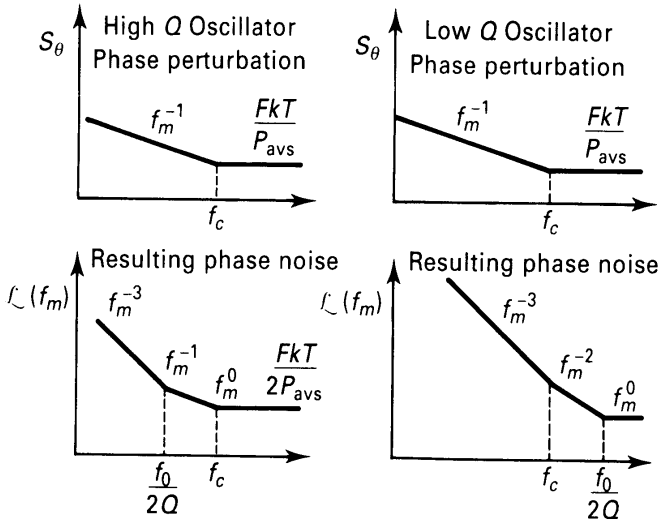


Figure 42--Oscillator phase noise for high-*Q* and low-*Q* resonators viewed as spectral phase noise and as carrier-to-noise ratio versus offset from the carrier.

3-2 Phase Noise in Frequency Dividers

In the previous picture showing the phase noise at the output frequency, we assumed that the only contributor is the frequency standard. Figure 43 shows the noise as a function of carrier

offset for different frequency dividers. The selection of the appropriate technology is very critical, and this plot does not have yet the relevant numbers for silicon-germanium (SiGe) technology based dividers, but it is unlikely that they are better than the 74AC series or the 74HC series devices. However, because of the frequency limitations of 74-series devices, we may not have that many choices. The GaAs divider, of course, is the noisiest one.

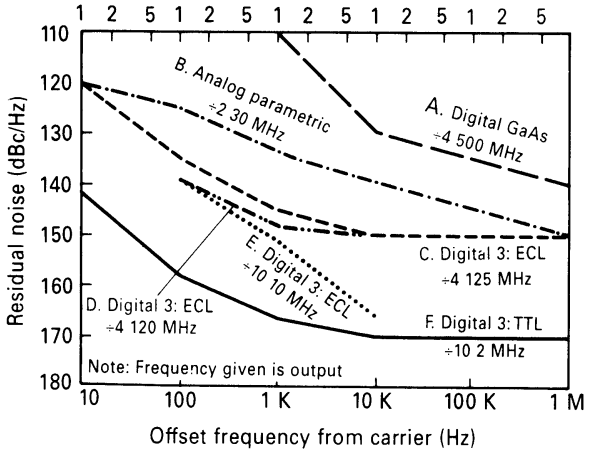


Figure 43--Residual phase noise of different dividers as a function of offset from the carrier frequency.

If we normalize the performance of the various dividers to 10 GHz, we can compare them much more easily. Figure 44 shows this comparison.

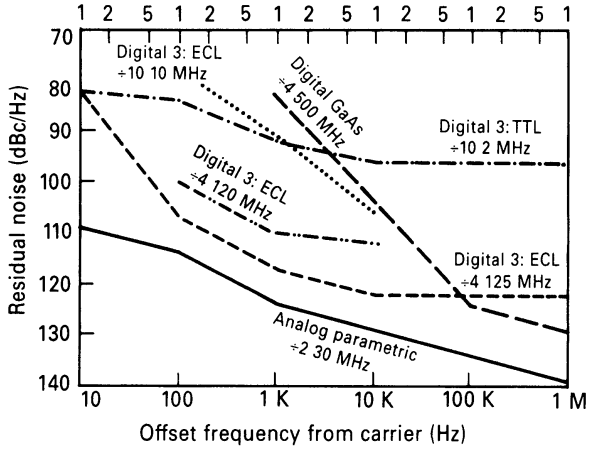


Figure 44--Phase noise of different dividers normalized to 10 GHz.

3-3 Noise in Phase Detectors

Phase detectors rarely operate above 50 MHz. Figure 45 shows the phase noise of an ECL phase/frequency discriminator and a diode ring. According to Goldberg [10], CMOS-based phase/frequency discriminator follows more the equation

$$\mathcal{L} = \mathcal{L}_0 + 10 \log(F_r) \tag{50}$$

where $\mathcal{L}_0$ is a constant that is equivalent to the phase/frequency detector noise with F_r = 1 Hz. $\mathcal{L}$ as a function of F_r is given below for standard PLL chips:

$\mathcal{L}$ (dBc/Hz)	F_r (Hz)
−168 to −170	10 k
−164 to −168	30 k
−155 to −160	200 k
−150 to −155	1 M
−145	10 M

The observant reader will notice that the CMOS phase/frequency discriminator seems to get worse with increasing offset from the carrier, while the plot in Figure 45 shows the opposite.

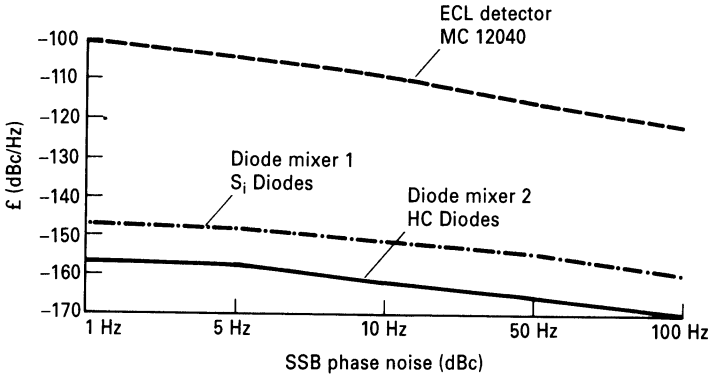


Figure 45--Phase noise of an ECL phase detector compared to a silicon-diode mixer and hot-carrier-diode (double-balanced) mixer.

3-4 Phase Noise in Diodes and Transistors

Diode Noise Model. The noise model for the diodes (Figure 46) consists of two contributions: the shot noise and the flicker noise. The shot noise is computed automatically and does not require any parameters. The flicker noise can be specified in two ways:

1. Using the enhanced SPICE noise model by specifying KF, AF, and FCP in the model parameter list (this option is usually sufficient for most applications).

2. Using bias-dependent flicker noise coefficients (specifying KF and AF at multiple bias points).

Diode Noise Model Keywords

keyword	**description**	**unit**	**default**
ID	**Required** bias current for the data point	Ampere	
KF	Flicker noise coefficient		0.0
AF	Bias exponent of the flicker noise model		1.0
FCP	Frequency exponent of the flicker noise model		1.0
FC	Flicker noise corner frequency	Hz	

The noise generators in the diode noise model are the series parasitic resistance, R_S, and the intrinsic junction. The figure below illustrates the intrinsic junction noise generator. Let Δf be the bandwidth (usually normalized to 1 Hz). The intrinsic noise generator has a mean-square value of:

$$\left\langle i_{Dn}^2 \right\rangle = 2qI_D\,\Delta f + \mathrm{KF}\frac{I_D^{\mathrm{AF}}}{f^{\mathrm{FCP}}}\Delta f \tag{51}$$

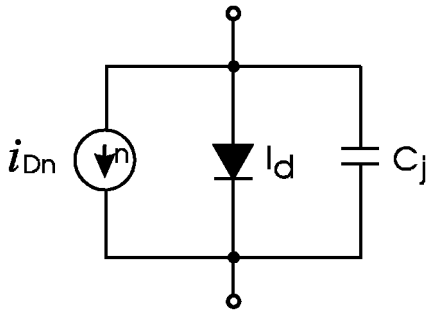


Figure 46--Equivalent noise circuit for a diode chip.

Notes on the Diode Noise Model:

1. Shot noise is always present unless the SN parameter is set to zero. Turning noise off is useful for comparing the total circuit noise that is generated by the nonlinear devices and that generated by the linear circuit components.

2. If the value of KF is specified as zero, then the flicker noise will not be contributed by the device and only shot noise is considered in the intrinsic model.

3. The corner frequency noise model uses the system noise floor to internally compute the flicker noise coefficient, KF. The system noise floor is computed by the program using the diode parameters and *kT*.

4. This noise model of course considers the actual operating temperature, which must be supplied to the model.

BJT Noise Model. The noise model for the Gummel-Poon BJT model consists of two contributions: shot noise and the flicker noise. The shot noise is computed automatically and does not require any parameters. The flicker noise can be specified in two ways:

1. Using the enhanced SPICE noise model by specifying KF, AF, and FCP in the model parameter list (this option is usually sufficient for most applications).

2. Using bias-dependent flicker noise coefficients (specifying KF and AF at multiple bias points).

Option 1: Specifying the Bias-Independent Flicker Noise Coefficient. This option involves the straightforward specification of KF, AF, and FCP that are constant with bias, as in the SPICE noise model. Notes on Option 1:

1. Shot noise is always present unless it is turned off. Turning noise off is useful for comparing the total circuit noise that is generated by the nonlinear devices and that generated by the linear circuit components.

2. If the value of KF is specified as zero, flicker noise will not be contributed by the device and only shot noise is considered in the intrinsic model.

Option 2: Specifying The Bias-Dependent Flicker Noise Coefficient or Flicker Corner Frequency

Option 2 allows a bias-dependent flicker noise coefficient (that is, KF and AF vary with the bias point).

BJT Noise Model Keywords

keyword	**description**	**unit**	**default**
IB	**Required** base bias current for the data point	ampere	
VCE	**Required** collector-emitter voltage for the data point	volt	
VBS	Base-substrate voltage required for LPNP type when four nodes are used.	volt	
VCS	Collector-substrate voltage required for NPN or PNP type when four nodes are used.	volt-	
KF	Flicker noise coefficient		0.0
AF	Bias exponent of the flicker noise model		1.0
FCP	Frequency exponent of the flicker noise model		1.0
FC	Flicker noise corner frequency	Hz	

Notes on the BJT Noise Model:

1. KF, AF, and FC can be specified as bias dependent. If only one set of noise data is specified, the corresponding bias point is not meaningful because all parameters are considered constant over all bias values. However, the bias point is needed for the program to identify the data as bipolar noise data.

2. The corner frequency noise model option uses the system noise floor to compute the flicker noise coefficient, KF. The system noise floor is computed by the program using the transistor parameters and *kT*.

3. This noise model of course considers the actual operating temperature, which must be supplied to the model.

Figure 47 shows the BJT noise model. Let Δf be the bandwidth (usually normalized to a 1-Hz bandwidth). The noise generators introduced in the intrinsic device are shown below, and have mean-square values of:

$$\left\langle i_{bn}^2 \right\rangle = 2qI_B\Delta f + \mathrm{KF}\frac{I_B^{AF}}{f^{FCP}}\Delta f \tag{52}$$

$$\left\langle i_{cn}^2 \right\rangle = 2qI_C\Delta f \tag{53}$$

$$\left\langle i_{R_{bb}}^2 \right\rangle = \frac{4kT}{R_{bb}}\Delta f \tag{54}$$

$$\left\langle i_{R_{e1}}^2 \right\rangle = \frac{4kT}{R_{e1}} \Delta f \tag{55}$$

$$\left\langle i_{R_{c2}}^2 \right\rangle = \frac{4kT}{R_{c2}} \Delta f \tag{56}$$

$$I_B = \frac{I_{bf}}{BF} + I_{le} \tag{57}$$

$$I_C = I_{cf} - I_{cr} \tag{58}$$

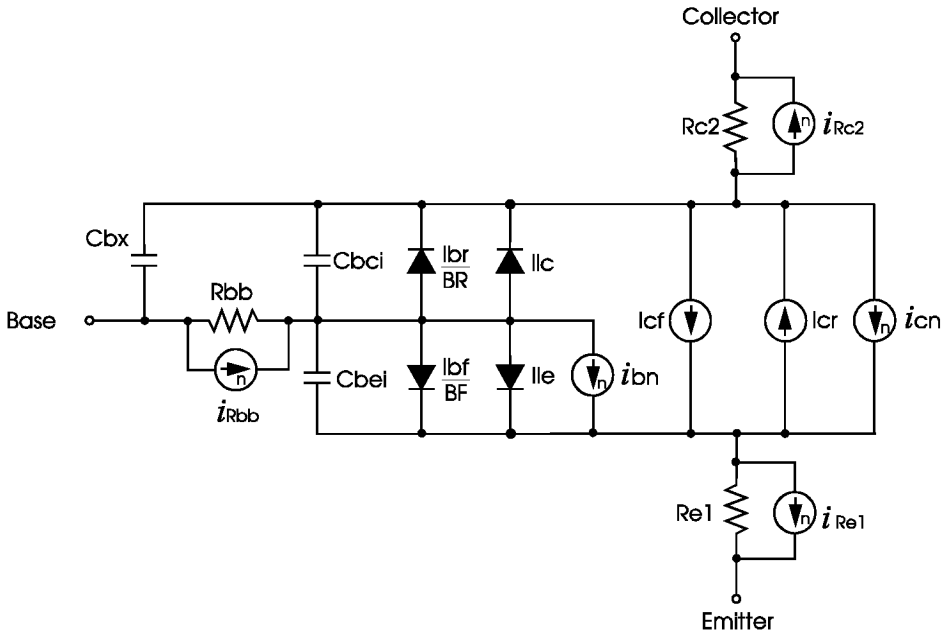


Figure 47--BJT noise model (not showing extrinsic parasitics). Current sources with n are noise sources.

JFET and MESFET Noise Model. The noise model for the FETs consists of two contributions: the shot noise and the flicker noise. There are two options to specify noise in the FET model:

1. Using the enhanced SPICE noise model by specifying KF, AF, and FCP in the model parameter list to determine the flicker noise (this option is usually sufficient for most applications). The shot noise will be automatically computed using the SPICE equation.

2. Using bias-dependent flicker noise coefficients through a reference in the DATA block (specifying KF and AF at multiple bias points) and specifying the four noise parameters ($F_{\min}$, MG_{opt}, PG_{opt}, and R_n) at multiple bias points.

Option 1: Specifying the Enhanced SPICE Noise Model. Option 1 is the straightforward specification of KF**,** AF, and FCP that are constant with bias, as in the SPICE noise model.

The drain noise model has the form:

$$\left\langle \left| I_{dn} \right|^2 \right\rangle = 4K_B T \frac{2g_m}{3} \Delta f + \mathrm{KF} \frac{\left| I_D \right|^{\mathrm{AF}}}{f^{\mathrm{FCP}}} \Delta f \tag{59}$$

where the shot noise is derived from g_m and the flicker noise is proportional to KF and the drain channel current, I_D, and inversely proportional to frequency. The AF and FCP parameters tailor the flicker noise dependence on bias and frequency, respectively.

Notes on Option 1:

1. Shot noise is always present unless it is turned off. Turning noise off is useful for comparing the total circuit noise that is generated by the nonlinear devices and that generated by the linear circuit components.

2. If the value of KF is specified as zero, then flicker noise will not be contributed by the device and only shot noise is considered in the intrinsic model.

(Option 2) Specifying The Bias-Dependent Flicker Noise Coefficient or Flicker Corner Frequency. Option 2 allows the specification of the complex bias-dependent nature of the shot noise and flicker noise. At high frequencies, the equivalent noise sources are correlated (the SPICE noise model does not account for this correlation). The complete evaluation of the shot noise sources can be determined from the four noise parameters. Since these are functions of bias, they can be specified over the (V_{GS}**,** V_{DS}) bias plane.

Additionally, a bias-dependent flicker noise coefficient (that is, KF and AF vary with current) can be specified.

The MESFET noise model uses the four measured noise data ($F_{\min}$, Γ_{opt}, and R_n) at one frequency and multiple arbitrary bias points. The program uses this data and the FET model parameters to de-embed the noise data to an intrinsic noise model. The intrinsic model is accurate at all frequencies, and therefore can predict the noise performance at all frequencies given data at just one frequency point. Built-in bias dependent characteristics are used if multi-bias noise data is not provided.

FET Noise Model Keywords

keyword	**description**	**unit**	**default**
FN	Noise data measurement frequency	Hz	1.0 GHz
VGS	**Required** gate-source voltage for the data point	volt	
VDS	**Required** drain-source voltage for the data point	volt	
FMIN	**Required** minimum noise figure in dB at FN		
MGO	**Required** magnitude of optimum noise reflectioncoefficient at FN		
PGO	**Required** phase of optimum noise reflection coefficient at FN		
RN	**Required** normalized noise resistance at FN		
KF	Flicker noise coefficient		0.0
AF	Bias exponent of the flicker noise model		1.0

FCP	Frequency exponent of the flicker noise model	1.0
FC	Flicker noise corner frequency	Hz

Notes on the FET noise model:

1. The corner frequency noise model option uses the system noise floor to compute the flicker noise coefficient, KF. The system noise floor is computed by the program using the transistor parameters and *kT*.

2. This noise model of course considers the actual operating temperature, which must be supplied to the model.

Noise in a MESFET is produced by sources intrinsic to the device. The same approach, but with different flicker corner frequencies, is highly applicable to JFETs and MOSFETs. For more detail as to simulation, see the Element library book for the active device portion of Ansoft's Serenade Design Environment product. The equivalent noisy circuit of an intrinsic FET is represented in Figure 48:

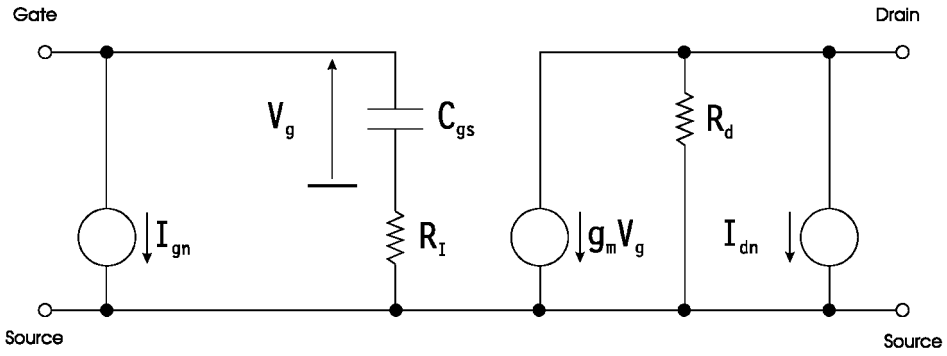


Figure 48--Equivalent noise circuit of an intrinsic FET device.

The intrinsic FET is internally represented as a noiseless nonlinear two-port with one equivalent noise current connected across the gate-source terminal, and one across the drain-source terminal. The correlations of the gate and drain noise current sources are:

$$\left\langle \left| I_{gn} \right|^2 \right\rangle = 4K_B T\Delta f \frac{w^2 C_{gs}^2}{g_m} R \tag{60}$$

$$\left\langle \left| I_{gn} \right|^2 \right\rangle = 4K_B T\Delta f g_m P \tag{61}$$

$$\left\langle I_{gn} I_{dn}^* \right\rangle = 4K_B T\Delta f j w C_{gs} \sqrt{PR}\, C \tag{62}$$

The correlation matrix of the noise current sources is

$$C_{dc}(w) = \frac{2}{p} K_B T dw \begin{bmatrix} \frac{w^2 C_{gs}^2}{g_m} R & -jwC_{gs}\sqrt{PR}\,C \\ jwC_{gs}\sqrt{PR}\,C & g_m P \end{bmatrix} \tag{63}$$

The gate and drain noise parameters R and P and the correlation coefficient C are related to the physical noise sources acting in the channel and are functions of the device structure and bias noise parameters. By defining measured noise parameters, $F_{\min}$, R_n and Γ_{opt}, and using a noise-de-embedding procedure, the parameters R, P, and C and the intrinsic noise correlation matrix of a FET device as functions of device bias are determined by the program.

In addition to the noise sources shown above, the flicker (1/f) noise can also be modeled by means of a noise current source connected in parallel with the intrinsic drain port. The flicker noise component in a narrow band, Δf, is expressed in the form

$$\left\langle \left| I_f \right|^2 \right\rangle = \mathrm{Q}\Delta f \frac{\left| I_D \right|^{\mathrm{AF}}}{f^{\mathrm{FCP}}} \tag{64}$$

where I_D is the instantaneous value of the channel current, and Q, AF, and FCP are empirical parameters. In most practical cases, AF and FCP are directly obtained from measurements (typically, AF = 2 and FCP = 1), while Q is not. In Ansoft's Serenade Design Environment, Q is either provided directly using KF or is computed by providing the flicker corner frequency (FC). FC is the frequency at which the flicker noise equals the shot/diffusion noise. The corner frequency is defined by the equation

$$\mathrm{Q}\frac{\left| I_D \right|^{\mathrm{AF}}}{f_{\mathrm{C}}^{\mathrm{FCP}}} = g_m P \tag{65}$$

Given the corner frequency FC and the measurement bias point V_{gs} and V_{ds}, the program automatically computes I_D, g_m, and P, and finally Q.

More information on FET noise modeling can be found in [11, 12, 13, 14, 15, 16, 17].

Scalable Device Models. Since diodes and transistors are scalable, here are guidelines for how to use scale them:

Microwave Diode

I_D = area × I_D
Cj = area × Cj
R_D = R_D / area

Bipolar Junction Transistor

I_{bf} = area × I_{bf} $\quad$ I_{br} = area × I_{br}
I_{le} = area × I_{le} $\quad$ I_{lc} = area × I_{lc}

I_{cf} = area × I_{cf}
C_{bc} = area × C_{bc}
C_{bx}= area × C_{bx}
RB2 = RB2 / area
RE1 = RE1 / area

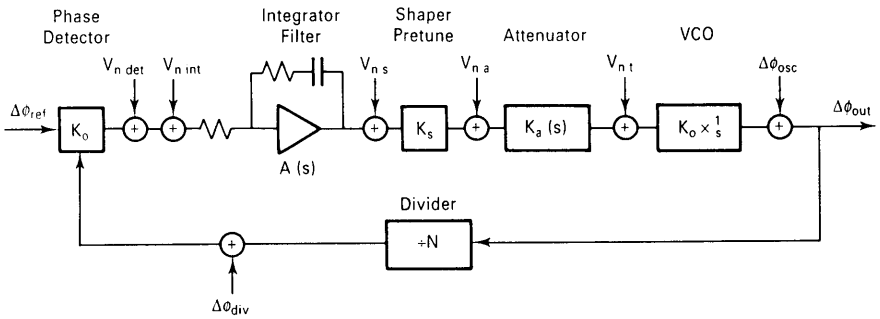
I_{cr} = area × I_{cr}
C_{be}= area × C_{be}
R_{bb} = R_{bb} / area
RC2 = RC2/ area
I_{jss} = I_{jss} × area
C_{jss} = C_{jss} × area

Materka FET

IGSS = IGSS × area
CGS0 = CGS0 × area
CGS1 = CGS1 × area
CDVC = CDVC × area
CDVS = CDVS × area
R_G = R_G × area / (number of fingers × 2)
R_D = R_D / area
R_S = R_S / area

3-5 Noise in Synthesizer Systems

The block diagram in Figure 49 shows a complete synthesizer in conventional (non-fractional-*N*) form. The reason why we exclude fractional-*N* has to do with the ΣΔ converters and other additional circuits that they require. I have already explained the noise components in fractional synthesizers; see Figure 29. Each of these components adds to the noise, and the list of recommendations guides how to minimize their impact or get the best overall noise performance.



Open Loop Gain : $G_{ol}(s) = K_\phi\, A(s)\, K_a(s)\, K_o\, \frac{1}{N}\, \frac{1}{s}$

- Minimize integrator, shaper, attenuator noise
- Maximize phase detector gain K_ϕ $\quad \frac{\Delta\phi_{out}}{V_{n\,int}} = \frac{1}{K_\phi} \frac{N}{1 + \frac{1}{G_{ol}(s)}}$
- Minimize sensitivity of VCO, K_o $\quad \frac{\Delta\phi_{out}}{V_{nt}} = \frac{\frac{K_o}{s}}{1 + G_{ol}(s)}$
- Employ attenuator and minimize $K_a(s)$

  e.g., effect of $V_{n\,int}$ (outside loop bandwidth) : $\Delta\phi_{out} = K_a(s)\, A(s)\, K_s\, K_o \frac{1}{s} V_{n\,int}$

Total response due to all noise excitations :

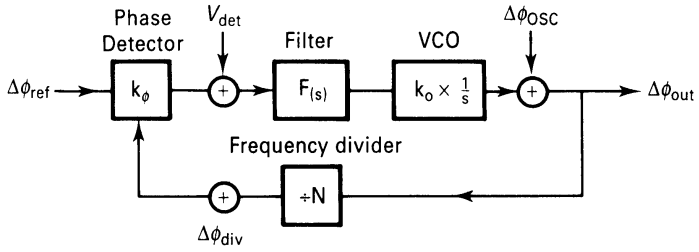
$$\Delta\phi^2_{out}(s) = \left(\frac{N}{1 + \frac{1}{G_{ol}(s)}}\right)^2 \left[\Delta^2\phi_{ref}(s) + \Delta^2\phi_{div}(s)\right]$$

$$+ \frac{1}{K^2_\phi}\left(\frac{N}{1 + \frac{1}{G_{ol}(s)}}\right)^2 \left[V^2_{n\,det}(s) + V^2_{n\,int}(s) + \frac{1}{A(s)^2} V^2_{ns}(s) + \frac{1}{A(s)^2}\frac{1}{K^2_s} V^2_{n\,a}(s)\right]$$

$$+ \left(\frac{1}{1 + G_{ol}(s)}\right)^2 \left[\left(\frac{K_o}{s}\right) V^2_{n\,t}(s) + \Delta\phi^2_{osc}(s)\right]$$

Figure 49--Calculation of all the noise excitation.

In simple terms, Figure 50 shows the parameters to be optimized for the best overall performance.



PARAMETERS TO OPTIMIZE FOR MINIMUM OUTPUT PHASE NOISE

- Minimize phase noise of free-running VCO

$$\frac{\Delta\phi_{out}}{\Delta\phi_{osc}} = \frac{1}{1 + G_{ol}(s)}$$

Open loop gain $G_{ol}(s) = k_\phi F_{(s)} k_o \frac{1}{s} \frac{1}{N}$

- Maximize bandwidth and open loop gain

$$\frac{\Delta\phi_{out}}{\Delta\phi_{ref}} = \frac{1}{1 + \frac{1}{G_{ol}(s)}}$$

Constraints: N × Reference phase noise
N × Divider phase noise
N × Phase detector noise
Filtering of f_{ref} and spurious on reference signal
Loop stability

- Avoid dividers if possible

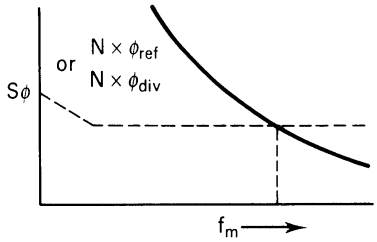


Figure 50--Parameters to be optimized for minimum output phase noise for phase-locked sources.

Figure 51 and 52 are good examples of a 10-GHz synthesized generator and a 47.104-GHz frequency source. A fairly large number of military applications and specifically some radar applications even use locked free-running oscillators rather than synthesizer/VCOs.

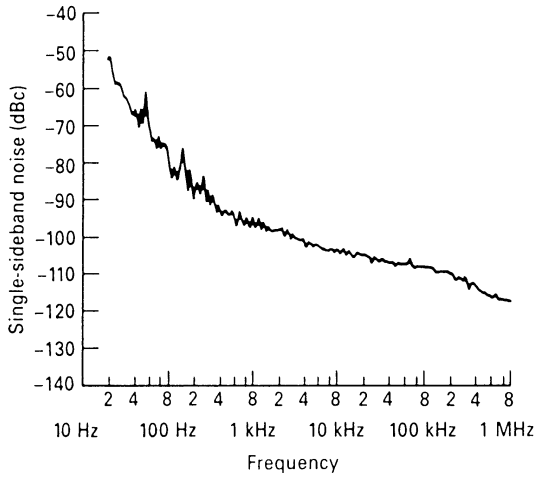


Figure 51--SSB phase noise of 10-GHz oscillator.

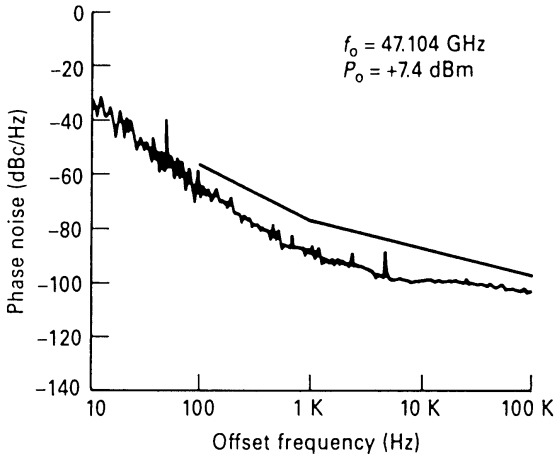


Figure 52--Measured phase noise of 47.104-GHz frequency source.

4 Summary

This presentation has provided some insight into the principles of phase-locked loops, specifically, the noise performance of oscillators, dividers, and phase/frequency discriminators. Guidelines have been established as to which components are critical, where the limits are, and how to select the optimum parameter values. The set of linear equations used are valid as long as the basic principle of the oscillator is being looked at. A more accurate prediction requires the use of a harmonic-balance simulator capable of predicting phase noise accurately. The presentation on oscillators from this morning, "Oscillator Basics and Low-Noise Techniques for Microwave Oscillators and VCOs," made extensive use of the appropriate CAD tool. It is necessary to finalize the prediction of the overall performance.

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