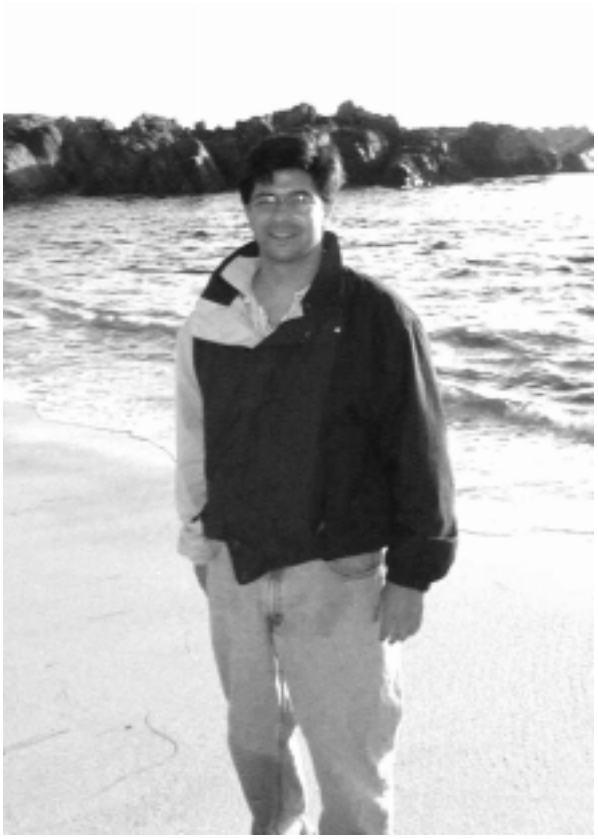
Message from the Author



I first became familiar with PLLs by working for National Semiconductor as an applications engineer. While supporting customers, I noticed that there were many repeat questions. Instead of creating the same response over and over, it made more sense to create a document, worksheet, or program to address these recurring questions in greater detail and just re-send the file. From all of these documents, worksheets, and programs, this book was born.

Many questions concerning PLLs can be answered through a greater understanding of the problem and the mathematics involved. By approaching problems in a rigorous mathematical way one gains a greater level of understanding, a greater level of satisfaction, and the ability to apply the concepts learned to other problems.

Many of the formulas that are commonly used for PLL design and simulation contain gross approximations with no or little justification of how they were derived. Others are rigorously derived, but from outdated textbooks that make assumptions not true of the PLL systems today. It is therefore no surprise that there are so many rules of thumb to be born which yield unreliable results. Another fault of these formulas is that many of them have not been compared to measured data to ensure that they account for all relevant factors.

There is also the other approach, not trusting formulas enough and trusting only measured results. The fault with this is that many great insights are lost and it is difficult to learn and grow in PLL knowledge this way. Furthermore, by knowing what a result should theoretically be, it makes it easier to spot and diagnose problems with a PLL circuit. This book takes a unique approach to PLL design by combining rigorous mathematical derivations for formulas with actual measured data. When there is agreement between these two, then one can feel much more confident with the results.

Credits

I would like to thank the following people for their assistance in producing this book.

Useful Insights: Ian Thompson (Phase Noise of the phase – frequency detector), Bill Keese (AN-1001/Loop Filter Design), Yuko Kanagy (General PLL)

Editing: Shigura Matsuda, Deborah Brown, Tom Mathews, Ahmed Salem
Bill Burdette (1st Edition)

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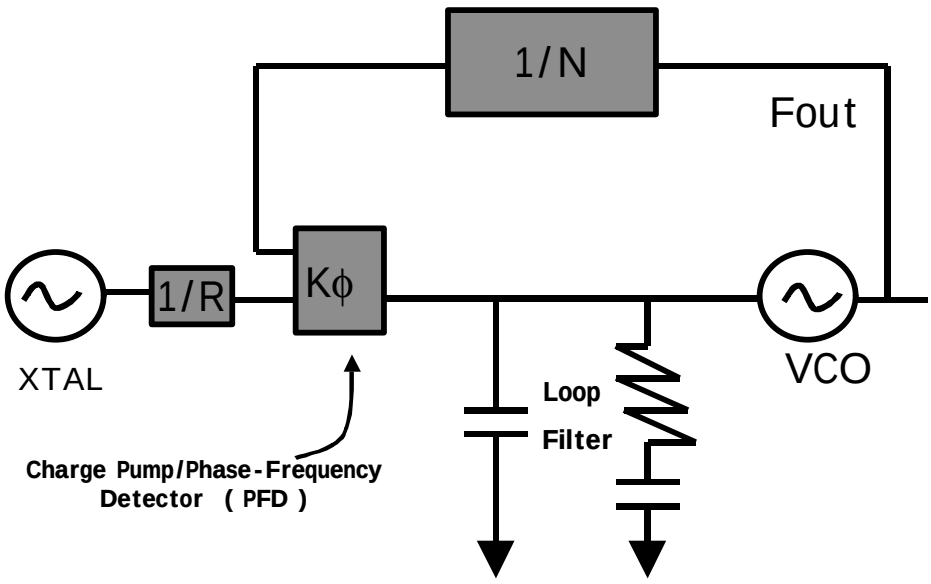


Figure 1 *The Basic PLL*

Basic PLL Operation and Terminology

This section describes basic ***PLL*** (Phased Locked Loop) operation and introduces terminology that will be used throughout this book. The PLL starts with a stable crystal reference frequency (***XTAL*)**. This frequency is divided by ***R*** to a lower frequency, which is called the comparison frequency (***Fcomp***). This is one of the inputs to the phase detector. The phase-frequency detector outputs a current that has an average DC value proportional to the phase error between the comparison frequency and the output frequency, after it is divided by the ***N*** divider. The constant of proportionality is called Kf. Note that this constant turns out to be the magnitude of the current that the charge pump can source or sink. Although it is technically correct to divide this term by 2π, it is unnecessary since it is canceled out by another factor of 2π which comes from the VCO gain for all of the equations in this book. So technically, the units of Kf are expressed in mA/(2π radians).

If one takes this average DC current value from the phase detector and multiplies it by the impedance of the loop filter (***Z(s)***), then the input voltage to the ***VCO*** (Voltage Controlled Oscillator) can be found. The VCO is a voltage to frequency converter and has a proportionality constant of ***Kvco***. Note that the loop filter is a low pass filter, often implemented with discrete components. This loop filter is application specific, and much of this book is devoted to the loop filter. This tuning voltage adjusts the output phase of the VCO, such that its phase, when divided by N, is equal to the phase of the comparison frequency. Since phase is the integral of frequency, this implies that the frequencies will also be matched, and the output frequency will be given by:

$$Fout = \frac{N}{R} \bullet XTAL$$

This applies only when the PLL is in the locked state; this does not apply during the time when the PLL is acquiring a new frequency. For a given application, R is typically fixed, and the N value can easily be changed. If one assumes that N and R must be an integer, then this implies that the PLL can only generate frequencies that are a multiple of ***Fcomp***. For this reason, many people think that ***Fcomp*** and the channel spacing are the same. Although this is often the case, this is not necessarily true. For a fractional N PLL, N is not restricted to an integer, and therefore the comparison frequency can be chosen to be much larger than the channel spacing. There are also less common cases where the comparison frequency is chosen smaller than the channel spacing to overcome restrictions on the allowable values of N, due to the prescaler. In general, it is preferable to have the comparison frequency as high as possible for optimum performance.

Note that the term PLL technically refers to the entire system shown in Figure 1; however, sometimes it is meant to refer to the entire system except for the crystal and VCO. This is due to the fact that these components are difficult to integrate on a PLL synthesizer chip.

The transfer function from the output of the R counter to the output of the VCO determines a lot of the critical performance characteristics of the PLL. The closed loop bandwidth of this closed loop system is referred to as the loop bandwidth (***wc***), which is an important parameter for both the design of the loop filter and the performance of the PLL. Another parameter, phase margin (***f***) refers to 180 degrees minus the phase of the open loop phase transfer function from the output of the R counter to the output of the VCO. The phase margin is evaluated at the frequency that is equal to the loop bandwidth. This parameter has less of an impact on performance than the loop bandwidth, but still does have a significant impact and is a measure of the stability of the system.

The PLL as a Frequency Synthesizer

The PLL has been around for many decades. Some of its earlier applications included keeping power generators in phase and synchronizing to the sync pulse in a TV Set. Still other applications include recovering a clock from asynchronous data and demodulating an FM modulated signal. However, the focus of this book is the use of a PLL as a frequency synthesizer.

In this type of application, the PLL is used to generate a set of discrete frequencies. A good example of this is FM radio. In FM radio, the valid stations range from 88 to 108 MHz, and are spaced 0.1 MHz apart. The PLL generates a frequency that is 10.7 MHz less than the desired channel, since the received signal is mixed with the PLL signal to always generate an IF (Intermediate Frequency) of 10.7 MHz. Therefore, the PLL generates frequencies ranging from 77.3 MHz to 97.3 MHz. The channel spacing would be equal to the comparison frequency, which would is 100 KHz.

A fixed crystal frequency of 10 MHz can be divided by an R value of 100 to yield a comparison frequency of 100 KHz. Then the N value ranging from 773 to 973 is programmed into the PLL. If the user is listening to a station at 99.3 MHz and decides to change the channel to 103.4 MHz, then the R value remains at 100, but the N value changes from 886 to 927. The performance of the radio will be impacted by the spectral purity of the PLL signal produced and also the time it takes for the PLL to switch frequencies.

The loop filter has a large impact on how long it takes for the PLL to switch frequencies and also on how spectrally pure the PLL signal produced is. For this reason, loop filter design is the central focus of this book.

ii. The Charge Pump PLL with a Passive Loop Filter

Why this Book Focuses on Charge Pump PLLs

This book is focused primarily on the charge pump PLL, since vast majority of PLLs available in the market today are of this type. The charge pump PLL offers many advantages over the classical voltage phase detector PLL including an infinite pull-in range and zero steady state phase error. Furthermore, there is already a considerable amount of literature that discusses features that are specific only to the voltage phase detector in great depth. By not focusing on the classical voltage phase detector, there is more time to focus on other features of the PLL. The charge pump PLL allows the use of a passive filter while still retaining the benefits of an active filter with the voltage phase detector. Passive filters are generally recommended, because they have the advantages of lower cost and no active devices to add noise. The exception to this case is when the VCO tuning voltage needs to be higher than the charge pump can supply – in this case, an active filter is necessary.

The Classical Voltage Phase Detector

In the past, active filters have been emphasized for several reasons that are explained in depth in Floyd Gardner's classical book, Phaselock Techniques. Many of these concepts still apply to the charge pump PLL, while many others, such as the steady state phase error are quite outdated. The XOR gate and the mixer are both discussed as practical ways to implement a phase detector. In Gardner's book, the following classical active loop filter topology is presented.

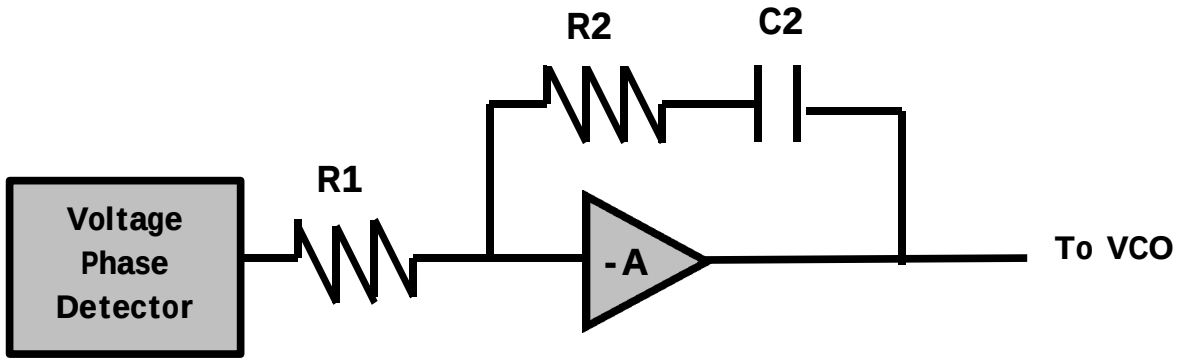


Figure 1 *Classical Active Loop Filter Topology for a Voltage Phase Detector*

The Modern Phase Frequency Detector with Charge Pump and its Advantages

The phase frequency detector with charge pump combination offers several advantages over the voltage charge pump and has all but replaced it. The phase-frequency detector and charge pump are usually integrated on the PLL chip. Using this approach completely eliminates the issues of steady state phase error and hold in range. The PLL with this combination can be compared to its predecessor as is done in Figure 2. Note that the circuit shown below with the box drawn around it integrates the functionality of the op-amp. It is necessary to divide the phase detector voltage gain (in Figure 1) by ***R1*** in order convert the voltage gain to a current gain.

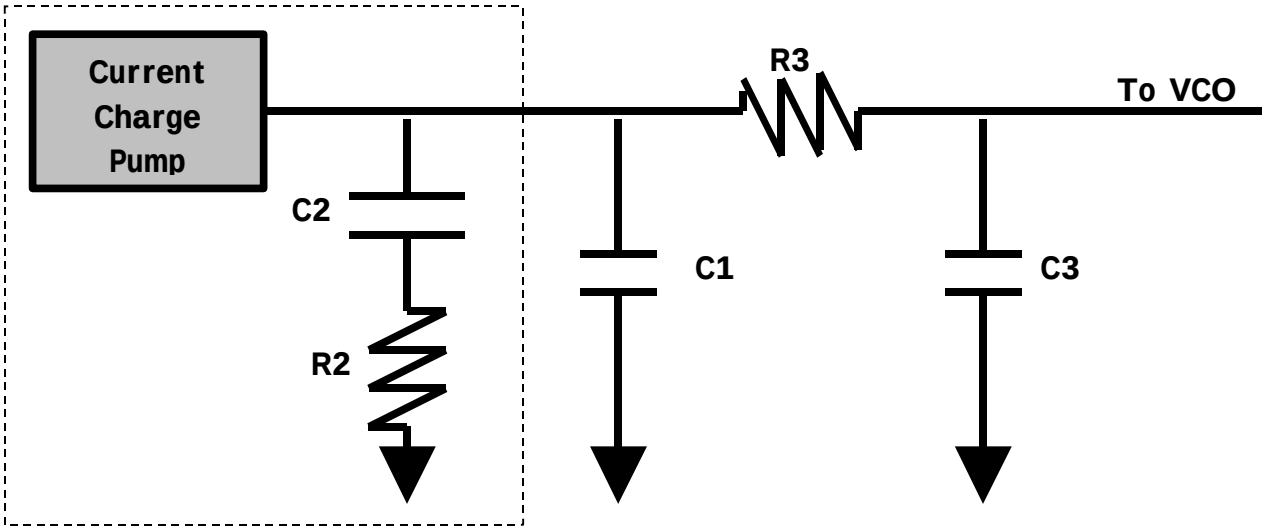


Figure 2 *Passive Loop Filter with Charge Pump*

The capacitor ***C1*** is added, because it reduces the spur levels significantly. Also, the components ***R3*** and ***C3*** can be added in order to further reduce the reference spur levels. Note that this passive filter has the op-amp functionality included. Instead of the phase detector delivering a voltage proportional to the phase error, the charge pump delivers a current with average value proportional to the phase error. This current is actually a constant amplitude with variable duty cycle. It is usually sufficient to model this current as an analog current with the average value proportional to the phase error. This is called the continuous time approximation and is used in most of the chapters in this book.

iii. The PLL as Viewed from a System Level

Introduction

This chapter discusses, on a very rudimentary level, how a PLL could be used in a typical wireless application. It also briefly discusses the impact of phase noise, reference spurs, and lock time on system level performance.

Typical Wireless Receiver Application

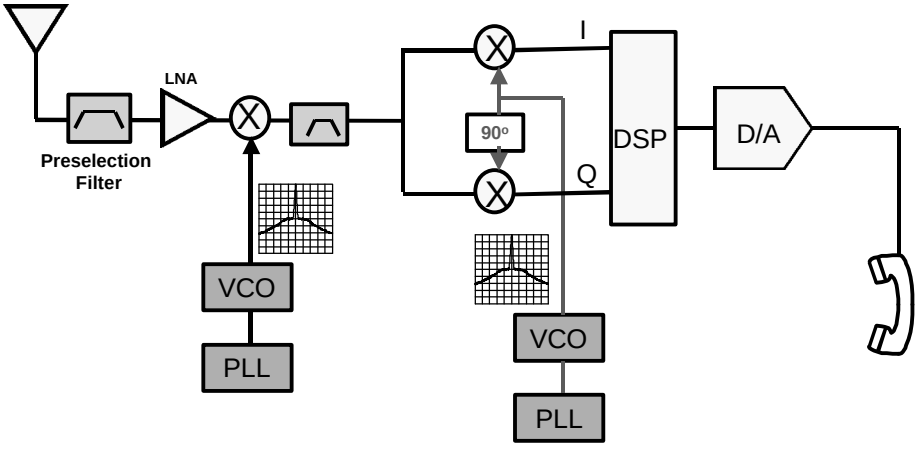


Figure 1 *Typical PLL Receiver Application*

General Receiver Description

In the above diagram, there are several different channels being received at the antenna, each one with a unique frequency. The first PLL in the receiver chain is tuned so that the output from the mixer is a constant frequency. The signal is then easier to filter and deal with since it is a fixed frequency from this point onwards, and because it is also lower in frequency. The second PLL is used to strip the information from the signal. Other than the obvious parameters of a PLL such as cost, size, and current consumption, there are three other parameters that are application specific. These parameters are phase noise, reference spurs, and lock time and are greatly influenced by the loop filter components. For this reason, these performance parameters are not typically specified in a datasheet, unless the exact application, components, and design parameters are known.

Phase Noise, Reference Spurs, and Lock Time as They Relate to This System

Phase noise refers to noise generated by the PLL. It can increase the bit error rates and the signal to noise ratio of the system. Reference spurs are unwanted noise sidebands that can occur at multiples of the comparison frequency , and can be translated by a mixer to the desired signal frequency. They can mask or degrade the desired signal. Lock time is the time that it takes for the PLL to change frequencies. It is dependent on the size of the frequency change and what frequency error is considered acceptable. When the PLL is switching frequencies, no data can be transmitted, so lock time of the PLL must lock fast enough as to not slow the data rate. Phase noise, reference spurs, and lock time are discussed in great depth in the rest of this book.

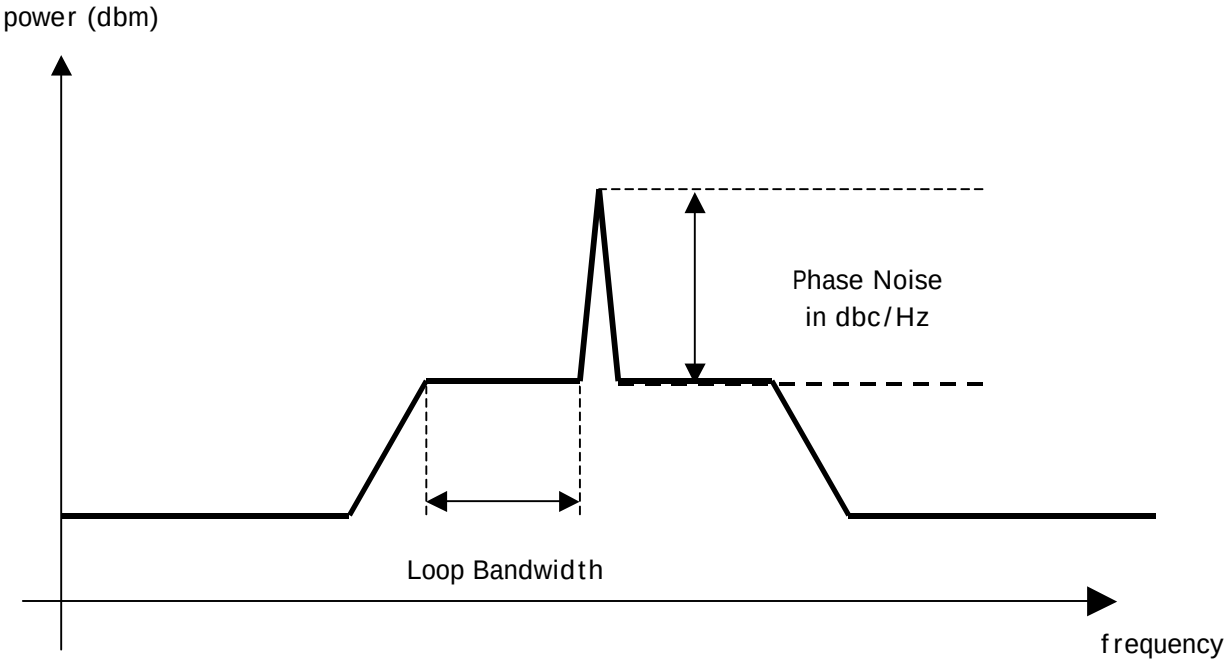
For the receiver shown in Figure 1, the first PLL that is closest to the antenna is typically the most challenging from a design perspective, due to the fact that it is higher frequency and is tunable. Since this PLL is tunable, there is typically a more difficult lock time requirement, which in turn makes it more challenging to meet spur requirements as well. In addition to this, the requirements on this PLL are also typically more strict because the undesired channels are not yet filtered out from the antenna.

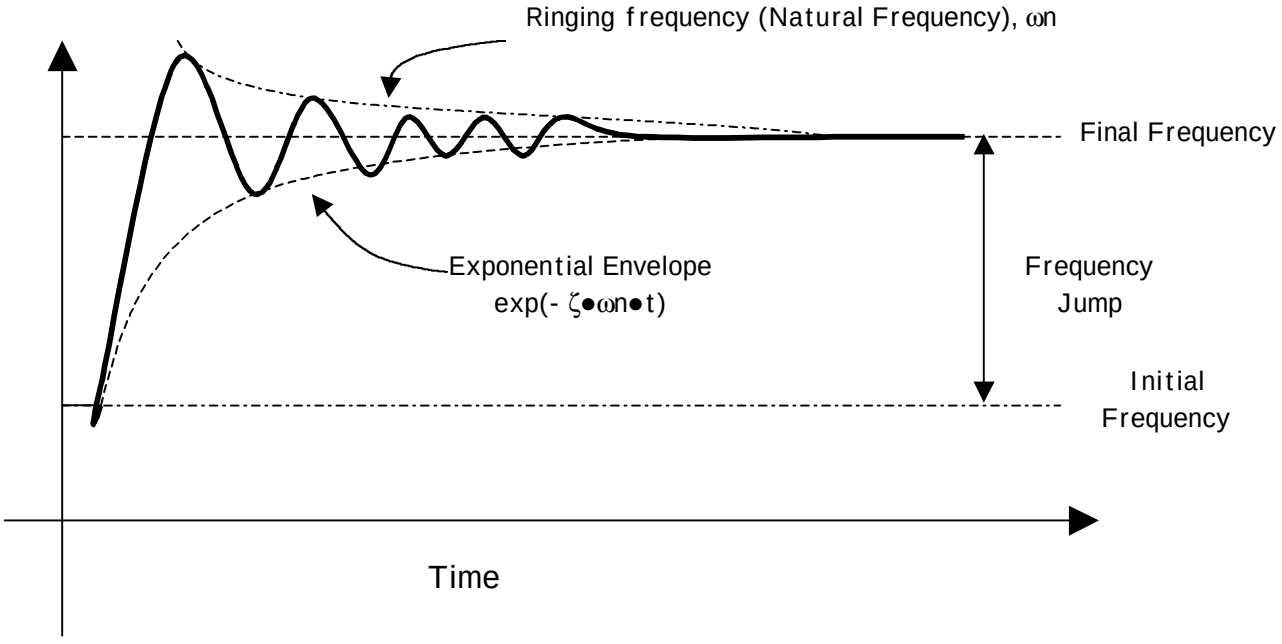
The second PLL has less stringent requirements, because it is lower frequency and also it is often not tunable. This makes lock time requirements easier to meet. There is also a trade off between lower spur levels and faster lock times for any PLL. So if the lock time requirements are relaxed, then the reference spur requirements are also easier to meet. Note also that since the signal path coming to the second PLL has already been filtered, the lock time and spur requirements are often less difficult to meet.

Conclusion

The PLL is a basic building block that can be used in just about any application where a frequency needs to be synthesized. It is the application that puts restrictions on phase noise, reference spurs, and lock time. These three performance parameters are greatly influenced by many factors including the VCO, loop filter, and N divider value.

PLL Performance and Simulation





1. Reference Spurs and their Causes

Introduction

In PLL frequency synthesis, reference sidebands and spurious outputs are an issue in design. There are several types of these spurious outputs with many different causes. However, by far, the most common type of spur is the reference spur. These spurs appear at multiples of the comparison frequency.

This chapter investigates the causes and behaviors of these reference spurs. In general, spurs are caused by either leakage or mismatch of the charge pump. Depending on the cause of the reference spurs, the spurs may behave differently when the comparison frequency or loop filter is changed. This chapter will discuss how to determine which is the dominant cause for a given application. In order to discuss spur levels, the fundamental concept of spur gain will be introduced. A clear understanding of spur gain is the starting point to understanding how reference spurs will vary from one filter to another. After this concept is developed, leakage and mismatch dominated spurs will be discussed, and then these results will be combined.

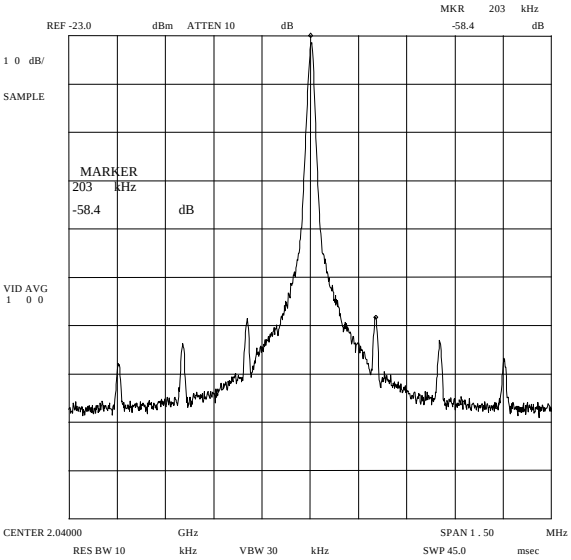


Figure 1 *Typical Reference Spur Plot*

The Definition of Spur Gain

Conceptually, if a given current noise of a fixed frequency is injected into the loop filter, then the power of the frequency noise that this induces at the VCO would be a start to defining the spur gain. However, an additional factor of ***1/s*** is included in the transfer function to simplify the arithmetic later. Note that since this is a frequency change, it is necessary to multiply the transfer function by a factor of ***s*** to convert from phase to frequency. This factor of ***1/s*** is left in, because it turns out that it is reintroduced because of other factors. Furthermore it makes the concept of spur gain a dimensionless quantity. Now since the power of the reference spur is sought, it is necessary to square this gain, and it is finally expressed in decibels for convenience.

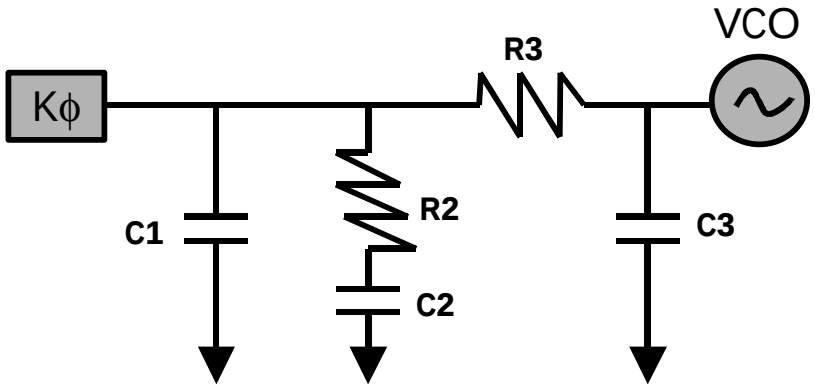


Figure 2 *Typical Third Order Loop Filter*

$$Spur\,Gain(\,Fspur\,) = 20 \bullet log\left(\left| \frac{Kf \bullet Z(s) \bullet Kvco}{s} \right|_{s = j \bullet Fspur \bullet 2 \bullet p} \right)$$

So spur gain is the product of the VCO gain, charge pump gain, and loop filter impedance evaluated at a frequency equal to the offset frequency of the spur of interest, ***Fspur***. In most cases, ***Fspur*** will be assumed to be the comparison frequency, ***Fcomp***, but it could also be other frequencies, such as multiples of the comparison frequency, or fractions of the comparison frequency (in the case of a fractional N PLL).

Aside from spur gain, there are other factors that contribute to spur levels, depending on whether the spurs are leakage dominated or mismatch dominated. The avid reader might wonder why the open loop transfer function is used, as opposed to the closed loop transfer function. In the case of leakage-dominated spurs, this would make sense, since it is the behavior the charge pump in the off state that causes the spurs. If the charge pump is off, it therefore makes sense to use the open loop transfer function. In the case of a mismatch-dominated spur, it may not be so obvious which transfer function to use. Since the open loop transfer function approximates the closed loop transfer function very well at the reference spurs frequencies, it makes most sense to use the open loop transfer function for the sake of consistency and simplicity.

Leakage Dominated Spurs

At lower comparison frequencies, leakage effects are the dominant cause of reference spurs. When the PLL is in the locked condition, the charge pump will generate short alternating pulses of current with long periods in between in which the charge pump is tri-stated.

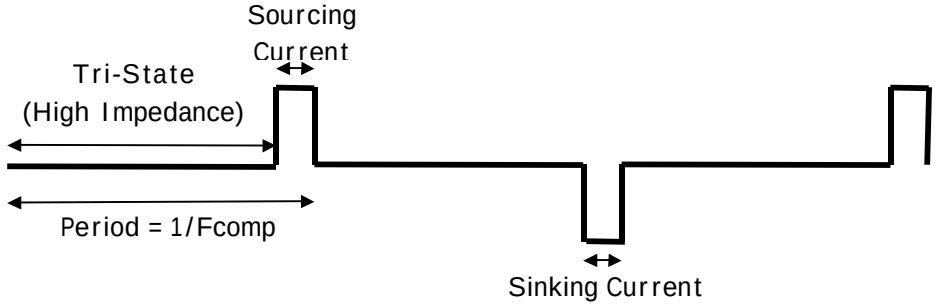


Figure 3 *Output of the Charge Pump When the PLL is in the Locked Condition*

When the charge pump is in the tri-state state, it is ideally high impedance. However, there will be some parasitic leakage through the charge pump, VCO, and loop filter capacitors. Of these leakage sources, the charge pump tends to be the dominant one. This causes FM modulation on the VCO tuning line, which in turn results in spurs. This is described in greater detail in the appendix.

To predict the reference spur levels based on leakage, use the following general rule:

$$Leakage\ Spur = BaseLeakageSpur + 20 \bullet log\left(\frac{Leakage}{Kf}\right) + Spur\ Gain$$

The leakage due to the PLL charge pump is temperature dependent and is often given guaranteed ratings as well as typical ratings and graphs in performance. The leakage of the charge pump increases with temperature, so spurs caused by leakage of the charge pump tend to increase when the PLL is heated.

Various leakage currents were induced at various comparison frequencies, and the results were measured on the bench. The loop filter was not changed during any of these measurements. These results imply the fundamental constant for leakage-dominated spurs:

$$BaseLeakageSpur = 16.0\ dBc$$

Note that this constant is universal and not part specific and should apply to any integer PLL. It can also not be stressed enough that it is impossible to directly measure the *BaseLeakageSpur* – this number is extrapolated from other numbers.

I_{leak} (nA)	20● Log (I_{leak} /Kϕ) (dB)	Fcomp (KHz)	Filter	Spur Levels (dBc)			Spur Gain (dB)			Implied BaseLeakage Spur (dbc)		
				1st	2nd	3rd	1st	2nd	3rd	1st	2nd	3rd
200	-86.0	50	A	-28.3	-40.5	-47.3	41.7	29.7	22.7	16.0	15.8	16.0
100	-92.0	50	A	-33.8	-45.7	-52.7	41.7	29.7	22.7	16.5	16.6	16.6
100	-80.0	100	B	-24.3	-40.5	-51.5	38.8	21.9	11.6	16.9	17.6	16.9
100	-80.0	200	B	-43.5	-61.5	-72.0	21.9	4.2	-6.3	14.6	14.3	14.3
500	-46.0	400	C	-32.7	X	X	-2.4	X	X	15.7	X	X
200	-54.0	400	C	-40.5	X	X	-2.4	X	X	15.9	X	X
Average Base Leakage spur										**15.9**	**16.1**	**16.0**

Filter	Kϕ (mA)	Kvco (MHz/V)	C1 (nF)	C2 (nF)	C3 (pF)	R2 (KΩ)	R3 (KΩ)	Output Frequency (MHz)
A	4.0	17	5.6	33	0	4.7	0	900
B	1.0	43	0.47	3.3	90	12	39	1960
C	0.1	48	1	4.7	0	18	0	870

Table 1 *Spur Level vs. Leakage Currents and Comparison Frequency*

Note that the ***BaseLeakageSpur*** index applies to the primary reference spurs as well as higher harmonics of this spur. Appendix B shows a theoretical calculation that is within 4 db of the measured results above. It is recommended that the measured value be used, since the theoretical derivation contains simplifying assumptions and may not account for all factors.

Pulse Related Spurs

In classical PLL literature, it is customary to model the reference spurs based entirely on leakage currents. For older PLLs, where the leakage currents were in the μA range, this made reasonable estimates for reference spurs and their behavior. However, modern PLLs typically have leakage currents of 1 nA or less, and therefore other factors tend to dominate the spurs, except at low comparison frequencies.

Recall that the charge pump comes on for very short periods of time and then is off during most of the time. It is the length of time that these short charge pump corrections are made that determines the pulse related spur. In other words, if leakage is not the dominant factor, then it is this time that the charge pump is on that determines the spur levels. There are several factors that influence this correction pulse width which include: charge pump mismatches, unequal transistor turn on times, dead-zone elimination circuitry, and inaccuracies in the fractional calibration circuitry. Below is an explanation of how these factors can influence the pulse width.

Mismatch of the charge pump refers to when the sink and source currents of the charge pump are not properly matched. The higher degree of the mismatch, the wider the correction pulse of the phase detector becomes. The unequal transistor turn on times refer to when the PMOS device that sources the current is not matched to the NMOS device that sinks the current. Since the PMOS process is slower, this typically makes it so that the lowest spur levels actually do not occur at 0% mismatch, but closer to about 4% mismatch. The dead zone elimination circuitry is added to keep the PLL out of the dead zone of the phase detector. Around zero phase error, real world issues of gate delays become a factor. To avoid this problem, circuitry can be added to ensure that the charge pump comes on for a minimum amount of time, which in turn impacts spur levels. Inaccuracies in the fractional calibration circuitry can also cause the fractional spurs to appear. All of these above sources increase the width of the charge pump correction pulse, so all of these effects contribute to the pulse spur.

For pulse related spur issues, it is important to be aware of the mismatch properties and to base the design around several different parts to get an idea of the full variations. Mismatch properties of parts can vary from date code to date code, so it is important to consider that in the design process. Also, in designs where an op-amp is used in the loop filter, it is best to use all of the tuning range of the PLL or to center the op-amp around half of the charge pump supply voltage or slightly higher. Due to this variation of spur level over tuning voltage to the VCO, the way that spurs are characterized in this chapter are by the worst case spur when the VCO tuning voltage is varied from 0.5 volts to 0.5 volts below the charge pump supply. The variation can also be mentioned, since this shows how much the spur varies, but ultimately, the worst case spur should be the figure of merit. To predict reference spurs caused by the pulsing action of the charge pump, the following rule applies.

$$\textit{Pulse Spur} = \textit{BasePulseSpur} + \textit{Spur Gain} + 40 \bullet \log\left(\frac{\textit{Fspur}}{1\ \textit{Hz}}\right)$$

The reader may be surprised to see that the above formula has the additional ***Fspur*** term added. This was first discovered by making observations with a modulation domain analyzer, which displays frequency versus time. In the case of the leakage-dominated spur, the VCO frequency was assumed to be modulated in a sinusoidal manner, which was confirmed with observations on the bench. However, this was not the case for the pulse-dominated spur. For these, frequency spikes occur a regular intervals of time corresponding to when the charge pump turns on. The pulse-dominated spurs were measured and their magnitude could be directly

correlated to the magnitude of these frequency spikes. This correlation was independent of the comparison frequency. Therefore, using the modulation index concept does not work for pulse dominated spurs and introduces an error equal to ***20●log(Fspur)***. However, the pulse spur differs from the leakage spur not by this factor but by ***40●log(Fspur).*** The additional factor of ***20●log(Fspur)*** comes because it is more proper to model the charge pump noise as a train of pulse functions, not a sinusoidal function. Recall to recover the time domain response of a pulse function applied to a system, this is simply the inverse Laplace transform. In a similar way that the inverse Laplace transform of ***1/s*** is just ***1***, and not involving any factors of ***1/w***, likewise in this situation, a factor of ***1/w*** is lost for this reason, thus accounting for the additional factor of ***40●log(Fspur).*** In the case of the LMX2350/52/54, these are the $1/16^{th}$ fractional spurs and have an additional dependence on the output frequency. This is due to the nature of the fractional spur compensation.

Fout MHz	N	Fspur KHz	Kϕ mA	Kvco MHz /V	C1 nF	C2 nF	C3 pF	R2 KΩ	R3 KΩ	Spur dBc	Spur Gain dB	BasePulse Spur dBc
This data was all taken from an LMX2330 PLL. The VCO was near the high end of the rail.												
1895	18950	100	4	43.2	2.2	10	0	6.8	0	-51.7	46	-297.7
1895	18950	100	4	43.2	13.9	66	0	2.7	0	-69.7	30	-299.7
1895	18950	100	4	43.2	0.56	2.7	0	15	0	-41.0	58	-299.0
1895	18950	100	4	43.2	1.5	6.8	0	5.6	0	-50.0	49.2	-299.2
1895	18950	100	4	43.2	1.5	6.8	100	5.6	39	-59.8	40.5	-300.3
1895	6064	312.5	4	43.2	4.7	20	0	1.8	0	-60.2	19.6	-299.6
1895	6064	3125.	4	43.2	1.8	5.6	0	1.5	0	-51.1	27.7	-298.6
This data was taken from an LMX2326 PLL with Vtune = 0.29 V and Vcc = 3 V												
231	1155	200	1	12	0.47	3.3	0	12	0	-74.1	23.0	-309.1
881.6	4408	200	1	18	0.47	3.3	0	12	0	-70.1	27.6	-309.7
881.6	1146	770	1	18	0.47	3.3	0	12	0	-70.1	4.9	-308.8
1885	9425	200	1	50	0.47	3.3	0	12	0	-59.7	35.6	-308.6
1885	4343	434	1	12	0.47	3.3	0	12	0	-58.7	22.2	-307.7

Table 2 *Demonstration of the Consistency of the BasePulseSpur*

The first several rows in Table 2 demonstrate many different filters at the same output frequency. The last several rows use the same filter, but emphasize the difference in changing the N value and comparison frequency. For the last several rows, the charge pump voltage was kept at 0.29 volts to maintain consistent mismatch properties of the charge pump and to also make spurs that were easy to measure. For this reason, this table is a valuable tool to show how spur levels vary. However, it is not a good source of information for worst case *BasePulseSpur*, since the tuning voltage was within 0.5 V of the supply rail and therefore out of specification.

PLL	Variation (dBc)	BasePulseSpur (dBc)
LMX2301/05, LMX2315/20/25	11	-299
LMX2330/31/32/35/36/37	23	-311
LMX2306/16/26	7	-309
LMX1600/01/02	5.0	-292
LMX2350/52/54	18	-257 – 40●log(Fout/1 GHz)

Table 3 *BasePulseSpur for Various National Semiconductor PLLs*

Despite the tables and measurements given above, the avid reader is sure to try to relate the pulse related spur to the mismatch of the charge pump. To do this, the LMX2315 PLL was used, and the spur level was measured along with the charge pump mismatch. The spur gain of this system was 19.6 dB, and in this system the comparison frequency was 200 KHz, so the spurs are clearly pulse-dominated.

Vtune (Volts)	1	1.5	2.2	3	4	4.5
Source (mA)	5.099	5.169	5.241	5.308	5.397	5.455
Sink (mA)	5.308	5.253	5.166	5.047	4.828	4.517
mismatch (%)	- 4.0	- 1.6	1.4	5.0	11.1	18.8
200 KHz Spur (dBc)	- 73.1	- 76.6	- 83.3	- 83.2	- 72.8	- 65.7

Table 4 *Sample Variation of Spur Levels and Mismatch with Do voltage*

Using statistical models, this suggests that the best spur performance is actually when the charge pump is 3.2 % mismatched and also gives the relationship:

$$BasePulseSpur = -315.6 + 1.28 \bullet |\, \%mismatch - 3.2\% \,|$$

Combining the Concepts of Leakage Related Spurs and Pulse Related Spurs

Critical Values for Comparison Frequency

In most cases, it makes sense to model the spurs as pulse related spurs, but this may not work for low comparison frequencies. One way to determine if a spur is leakage or pulse related is to calculate spurs based on both methods, and use whichever method yields the largest spur levels. In most cases, the pulse related spur will dominate. If the leakage is known, and the *BasePulseSpur* is known, it is possible to predict the comparison frequency for which the spur is equally pulse and leakage dominated. If the comparison frequency is higher than this, then the spur becomes more pulse dominated. Note that this calculation is independent of the spur gain and is found by setting the leakage spur equal to the pulse spur and solving for the comparison frequency. The governing equation and table for this are given below:

$$40 \bullet \log\left(\frac{Fcomp}{1\,Hz}\right) = \left(BaseLeakageSpur - BasePulseSpur\right) + 20 \bullet \log\left(\frac{leakage}{Kf}\right)$$

Comparison frequencies that satisfy this equation will be called critical frequencies. At the critical frequency, the reference spur is equally dominated by leakage and pulse effects. Above the critical frequency, the spur becomes more pulse dominated, below the critical frequency, the spur becomes more leakage dominated. This table was generated assuming the following:

$$BaseLeakageSpur = 16.0\ dBc$$
$$Kf = 1\ mA$$

Note that the critical frequency is proportional to the square root of the leakage current, and inversely proportional to the square root of the charge pump gain.

	BasePulseSpur			
	-290	***-300***	***-310***	***-320***
leakage = 0.1 nA	14.1	25.1	44.7	79.4
leakage = 0.5 nA	31.6	56.2	99.9	177.6
leakage = 1.0 nA	44.7	79.4	141.2	251.2
leakage = 0.1 uA	446.7	794.3	1412.5	2511.9
leakage = 1.0 uA	1412.5	2511.9	4466.8	7943.3

Table 5 *Critical Values for Comparison Frequency in Kilohertz*

Composite Spur Calculation

This chapter has independently derived the spur levels based on leakage and pulse effects. However, regardless of the dominant cause, the spur level is given by:

$$Spur = 10 \bullet \log\left(10^{Leakage\ Spur/10} + 10^{Pulse\ Spur/10} \right)$$

Spur Levels vs. Unoptimized Loop Filter Parameters

Using the expression for spur gain, the way that spur levels vary vs. various parameters can easily be calculated and is shown below:

Relationship to Parameter	Leakage Dominated Spurs	Pulse Dominated Spurs
Charge Pump Leakage, i_{leak}	20●log(i_{leak})	N/A
Mismatch, M	N/A	Correlated to | M - δ |
N Value, N	independent	independent
VCO Gain, Kvco	20●log(Kvco)	20●log(Kvco)
Comparison Frequency	-40●log(Fcomp)	-20●log(Fcomp)
i = Fcomp/Fc	-40●log(i)	-40●log(i) + 20●log(Fcomp)
Charge Pump Gain, Kf	independent	20●log(Kϕ)
Spur Gain, SG	SG	SG

Table 6 *Approximate Relationship of Spur Levels to Various Parameters Assuming that the Loop Filter is NOT Redesigned to Adjust for the Changed Parameter.*

Harmonics of Pulse Dominated Reference Spurs

In the case of a leakage-dominated spur, ***BaseLeakageSpur*** also applies to the spur harmonics, so this topic has already been covered. However, this case has not been treated in the case of pulse spurs. In order to address this issue, a LMX2326 PLL was tuned in 1 MHz increments from 1900 MHz to 1994 MHz using an automated test program. For these tests, Kϕ = 1 mA, Fcomp = 200 KHz, and Kvco = 45 MHz/V. Filter A had components of C1 = 145 pF, C2 = 680 pF, R2 = 33 KΩ, while Filter B had components of C1 = 315 pF, C2 = 1.8 nF, and R2 = 18 KΩ. The statistics for the spur levels are presented in Table 7a.

	Fundamental (200 KHz)	2nd Harmonic (400 KHz)	3rd Harmonic (600 KHz)
Minimum (dBc)	-56.2	-65.1	-64.5
Average (dBc)	-52.8	-58.5	-61.9
Maximum (dBc)	-49.3	-54.4	-59.0
Spur Gain for Spur (dB)	45.7	33.8	26.8
BasePulseSpur (dBc)	-307.0	-312.4	-316.9

Table 7a *Reference Spurs and their Harmonics for Filter A*

	Fundamental (200 KHz)	2nd Harmonic (400 KHz)	3rd Harmonic (600 KHz)
Minimum (dBc)	-64.8	-70.4	-69.1
Average (dBc)	-60.8	-65.1	-66.8
Maximum (dBc)	-56.2	-61.1	-64.7
Spur Gain for Spur (dB)	39.0	27.1	20.0
BasePulseSpur (dBc)	-307.2	-312.2	-315.8

Table 7b *Reference Spurs and their Harmonics for Filter B*

Table 7a to Table 7b show that the pulse spur is relatively consistent for different filters, however the second harmonic has a different BasePulseSpur than the first. These empirical measurements would suggest to expect that the BasePulseSpur for the second harmonic to be about 5 dB better than the BasePulseSpur for the first harmonic, and for the BasePulseSpur of the third harmonic to be about 4 dB better than the BasePulseSpur for the second harmonic.

Now Tables 7a and 7b show harmonics of pulse dominated reference spurs. Similar measurements can also be made for harmonics of leakage-dominated spurs. Theoretically, one would expect that the higher harmonics to behave differently than the fundamental leakage dominated spur, since they are based on the higher powers of the modulation index (See Appendix A), however measured results show that they can be treated just as the fundamental leakage spur, except for the value of BaseLeakageSpur for them is a little different.

	Fundamental (200 KHz)	2nd Harmonic (400 KHz)	3rd Harmonic (600 KHz)
Minimum (dBc)	-56.2	-65.1	-64.5
Average (dBc)	-52.8	-58.5	-61.9
Maximum (dBc)	-49.3	-54.4	-59.0
Spur Gain for Spur (dB)	45.7	33.8	26.8
BasePulseSpur (dBc)	-307.0	-312.4	-316.9

Table 7a *Reference Spurs and their Harmonics for Filter A*

Conclusion

This chapter has discussed the causes of reference spurs and given some techniques to simulate their general behavior. The concept of spur gain applies to reference spurs and gives a relative indication of how they vary from one loop filter to another when the other parameters, such as comparison frequency are held constant. Reference spurs can be caused by leakage or pulse effects. Pulse effects is a generic term to refer to inconsistencies in the pulse width of the charge pump caused by mismatch, unequal transistor turn on times, or imperfections in the fractional N compensation circuitry. Although reference spurs are intended to refer to spurs that

appear at a spacing equal to the comparison frequency from the carrier, the models in this chapter are also useful in predicting harmonics of reference spurs and fractional spurs. One caution dealing with fractional spurs is they may be sensitive to voltage and prescaler. They also often have a dependence on the output frequency as well. In general, the spur that is closest to the carrier is the most troublesome, since it is most difficult to filter.

As for the accuracy of the formulas presented in this chapter, there will always be some variation between the actual measured result and the theoretical results. Relative comparisons using spur gain tend to be the most accurate. In the case of leakage-dominated spurs, there is a discrepancy between the theoretical and empirical values for ***BaseLeakageSpur*** of about 4 db. It is recommended to use the empirical value, but to accept that there could be several dB variation between the predicted and measured results. In the case of pulse-dominated spurs, the value for ***BasePulseSpur*** is purely empirical and is based solely on measured data. These spurs can also change a good 15 dB as the VCO is tuned across its tuning range. However, the worst case spur is the one that is being modeled.

Appendix A: Spectra of Spurious Signals

Introduction

This section investigates the causes of spurs and their spectral density for an arbitrary time-varying signal that is fed to a VCO. It assumes a sinusoidal signal and is therefore meaningful in analyzing leakage-dominated spurs.

Derivation of Spurious Spectrum

Spurs are caused by the PLL when a signal with an AC component is presented to the tuning line of the VCO. Assume that the tuning voltage to the VCO has the form:

$$V_{tune} = V_{DC} + V_{AC}(t)$$

Where

V_{tune}	=	Tuning voltage to the VCO
V_{DC}	=	DC component of tuning voltage to the VCO
V_{AC}	=	AC component of tuning voltage to the VCO
	=	$V_m \bullet sin(w_m \bullet t)$
ω_m	=	Modulating Frequency = ***Fcomp***

The VCO has an output voltage of the form [1]:

$$V(t) = A \bullet cos[w_0 \bullet t + b \bullet sin(w_m \bullet t)]$$

Where

w_0	=	Carrier Frequency
b	=	Modulation Index

Since $b \bullet sin(w_n \bullet t)$, represents the phase deviation of the signal, this expression can be differentiated to determine the maximum frequency deviation, ***DF***, and the following identity can be derived [1]:

$$b = \frac{DF}{w_n}$$

By writing down the Fourier Series for $e^{j \bullet b \bullet sin(w_n \bullet t)}$, the following identity can be derived [1].

$$e^{j \bullet b \bullet sin(w_n \bullet t)} = \sum_{n=-\infty}^{\infty} J_n(b) \bullet e^{j \bullet n \bullet w_m \bullet t}$$

In the above expression, $J_n(b)$ is the Bessel function of the first kind of order ***n***.

Applying the identity allows the power spectral density to be simplified as follows [1].

$$\begin{aligned} Vout(t) &= A \bullet \cos\left[w_0 \bullet t + b \bullet \sin(w_m \bullet t)\right] \\ &= A \bullet Real\left\{ e^{j \bullet w_0 \bullet t} \sum_{n=-\infty}^{\infty} J_n(b) \bullet e^{j \bullet n \bullet w_m \bullet t} \right\} \\ &= A \bullet \sum_{n=-\infty}^{\infty} J_n(b) \bullet \cos(w_0 \bullet t + n \bullet w_m \bullet t) \end{aligned}$$

From this expression, the sideband levels can be found by visual inspection.

$$\begin{aligned} Carrier: &\quad J_0(b) \approx 1 \\ First: &\quad J_1(b) \approx \frac{b}{2} \\ Second: &\quad J_2(b) \approx \frac{b^2}{8} \\ n^{th}: &\quad J_n(b) \end{aligned}$$

Below is a table of first sideband level versus frequency deviation from zero for various comparison frequencies:

Spur Level (dBm)	Modulation Index (β)	Frequency Deviation for Various Comparison Frequencies (Hz)					
		Fcomp 10 KHz	*Fcomp 30 KHz*	*Fcomp 50 KHz*	*Fcomp 100 KHz*	*Fcomp 200 KHz*	*Fcomp 1000 KHz*
-30	6.32e-2	632	1900	3160	6320	12600	63200
-40	2.00e-2	200	600	1000	2000	4000	20000
-50	6.32e-3	63	190	316	632	1260	6320
-55	3.56e-3	36	107	178	356	712	3560
-60	2.00e-3	20	60	100	200	400	2000
-65	1.12e-3	11	34	56	112	224	1120
-70	6.32e-4	6	19	32	63	126	632
-75	3.56e-4	4	11	18	36	71	356
-80	2.00e-4	2	6	10	20	40	200
-85	1.12e-4	1	3	6	11	22	112
-90	6.32e-5	0.6	2	3	6	13	63

Table 7 *Relationship Between Spur Level, Modulation Index, and Frequency Variation*

The spur levels relate the modulation index by:

$$Spur\ Level = 20 \bullet \log(b/2)$$

References

[1] Tranter, W.H. and R.E. Ziemer *Principles of Communications Systems, Modulation, and Noise*, 2nd ed, Houghton Mifflin Company, 1985

Appendix B: Theoretical Calculation of Leakage Based Spurs

Since the ***BaseLeakageSpur*** is theoretically independent of PLL and loop filter, it makes sense to choose the loop filter that is the most basic. A simple capacitor is the most basic loop filter. Note that this filter topology is not a stable one, but for the purposes of this calculation, it will do just fine. Using this simplified loop filter, the voltage deviation to the VCO can easily be calculated.

$$\frac{DV}{Dt} = \frac{i}{C1}$$

Substituting in known values gives the voltage deviation.

$$DV = \int_0^{1/Fcomp} \frac{i}{C1} \bullet dt = \frac{i}{C1 \bullet Fcomp}$$

Now recall that this is the amount the voltage changes during one charge pump cycle. So to get the modulation index, it is necessary to divide by two. Therefore, the modulation index is:

$$b = \frac{Kvco \bullet DV}{2 \bullet Fcomp}$$

$$Leakage\ Spur = 20 \bullet \log\left(b/2\right)$$

Table 8 shows the fundamental result and how it can be derived. This number is within a few dB of what has been measured in practice.

Specified Quantities			Derived Quantities	
C1	10 nF		***Spur Gain***	8.073 dB
C2	0 nF		***DV***	1.000 μV
R2	0 KΩ		***b = modulation index***	0.00005
Kf	1 mA		***Leakage Spur***	= 20●log(β/2) = -92.041 dBc
Kvco	10 MHz/V		***20●(Leakage/Kf)***	-120.000
Leakage	1 nA		***BaseLeakageSpur***	= -92.0 dBc – (-120 dB) – 8.1 dB = **19.886 dBc**
Fcomp	100 KHz			

Table 8 *Theoretical calculation for BaseLeakageSpur = 19.9 dBc/Hz*

2. On Non-Reference Spurs and their Causes

Introduction

Much has been said about reference spurs, which occur at the reference frequency away from the carrier. This chapter investigates other types of spurs and their causes. The value of doing this is so that when a spur is seen, its causes and fixes can be investigated. Although many types of spurs are listed, most of these spurs are not usually present. Since a lot of these spurs occur in dual PLLs, the main PLL will always refer to the side of a dual PLL on which the spur is being observed, and the auxiliary PLL will refer to the side of a dual PLL that is not being observed. This chapter discusses general good tips for dealing with spurs, and then goes into categorizing the most common types, their causes, and their cures.

Tips for Good Decoupling and Good Layout

To deal with board-related cross talk, there are several steps that can be taken. Be sure to visit wireless.national.com and download the evaluation board instructions to see typical board layouts. In addition to this, there are the following additional suggestions:

Good Decoupling: By this it is meant to have several capacitors on both the VCC and charge pump supply lines. The charge pump supply lines are the most vulnerable to noisy signals. Place a 100 pF, 0.01 μF, and a 0.1 μF capacitor on each of these lines to deal with noise at a wide range of frequencies. It may seem that these capacitances simply add in parallel to form a 0.111 μF capacitor, but in fact, they are all necessary since the larger capacitors have more problems responding to high frequency signals and may have a higher ESR. It is also good to place these components as close to the PLL chip as possible. Also it is often good to isolate the power supply pins with a small resistor of about 18 Ω .

Good Layout: Be sure to protect the charge pump supply lines and the VCO tuning voltage lines from noisy signals. This can be done by making these traces short and as close as possible to the PLL chip. When two high frequency traces must be placed together, try to make them so that they are not parallel (i.e. try to make them perpendicular) in order to minimize the cross talk effects. Also try to minimize ground looping, which occurs when there is a small impedance (such as the inductance caused by a via) that connects two traces to ground. In the instance of ground looping noise can travel from one trace to another. Placing a ground plane in the board to separate the top and bottom layer also can help reduce cross talk effects.

Good Loop Filter Design: Higher order loop filters and filters with narrower loop bandwidth are more effective in reducing spurs of all sorts – not just reference spurs.

Cross Talk vs. Non-Cross Talk Related Spurs

For the purposes of this discussion, the spurs will be divided into two categories. Cross talk related spurs refer to any spur that is caused by some source other than the PLL that finds its way to VCO output. Non-cross talk related spurs refer to spurs that are caused by some inherent behavior in the PLL. The first step in diagnosing a spur is to determine whether or not it is a cross talk related spur. The way that this is done is by eliminating all potential causes of the cross talk spur and checking if the spur goes away.

Cross Talk Related Spurs

In general, signals that are either low frequency, or close to the PLL output frequency are the most likely to cause this type of spurs. Whenever two sinusoidal signals enter a non-linear device an output signal at the sum and the difference of these frequencies will be produced. This result can be derived by writing the first three general terms for the Taylor series and observing that the square term gives rise to these sum and difference frequencies. It therefore follows that frequencies that are low in frequency, or frequencies that are close to the PLL output frequency are the ones that cause the most problems with cross talk related spurs. Several different types of the cross talk related spur are given below:

External Cross Talk Spur

Description: This spur appears and is unrelated to the auxiliary PLL output. Often times, when the main PLL is tuned to different frequencies, this spur moves around.

Cause: This type of spur is caused by some frequency source external to the PLL. Common external sources that can cause these spurs are: computer monitors (commonly causes spurs at the screen refresh rate of 30 – 50 KHz), phones of all sorts, other components on the board, florescent lights, power supply (commonly causes spurs in multiples of 60 Hz), and computers. Long signal traces can act as an antenna and agitate this type of spur.

Diagnosis: To diagnose this spur, start isolating the PLL from all potential external noise sources. Switch power supplies. Turn off computer monitors. Go to a screen room. Disconnect the auxiliary VCO and power down the auxiliary PLL. By trial and error, external noise sources can be ruled out, one by one.

Cure: To eliminate this spur, remove or isolate the PLL from the noise source. As usual, these spurs are layout dependent, so be sure to read the section on good layout. Also consider using RF fences to isolate the PLL from potential noise sources.

Auxiliary PLL Cross Talk Spur

Description: This spur only occurs in dual PLLs and is seen at a frequency spacing from the carrier equal to the difference of the frequencies of the main and auxiliary PLL (or sometimes a higher harmonic of the auxiliary PLL). This spur is most likely to occur if the main and auxiliary sides of a dual PLL are close in frequency. If the auxiliary PLL is powered down, but the auxiliary VCO is running, then this spur can dance around the spectrum as the auxiliary frequency VCO drifts around.

Cause: Parasitic capacitances on the board can allow high frequency signals to travel from one trace on the board to another. This happens most for higher frequencies and longer traces. There could also be cross talk within the chip. The charge pump supply pins are vulnerable to high frequency noise.

Diagnosis: One of the best ways to diagnose this spur is to tune the auxiliary side of the PLL while observing the main side. If the spur moves around, that is a good indication that the spur being observed is of this type. Once this type of spur is diagnosed, then it needs to be determined if the spur is related to cross talk on the board, or cross talk in the PLL. Most PLLs

have a power down function that allow one to power down the auxiliary side of a PLL, while keeping the main side running. If the auxiliary side of the PLL is powered down, and the spur reduces in size substantially, this indicates cross talk in the PLL chip. If the spur stays about the same magnitude, then this indicates that there is cross talk in the board.

Cure: Read the section on how to deal with board related cross talk.

Crystal Reference Cross Talk Spur

Description: This spur is visible at an offset from the carrier equal to some multiple of the crystal reference frequency. Often times, there is a whole family of spurs that often occur at harmonics of the crystal reference frequency. In this case, the odd harmonics are usually stronger than the even harmonics.

Cause: This spur can be caused by excessive gain of the inverter in the crystal oscillator. Sometimes, this inverter is integrated unto the PLL chip. When any oscillator has excessive gain, it can give rise to harmonics. The reason that the odd harmonics are often stronger is that the oscillator often produces a square wave or a clipped sine wave, which has stronger odd harmonics. Figure 1 shows a the structure of a typical crystal oscillator. Note that ***Lm*** (motional inductance), ***Cm*** (motional capacitance), and ***Cp*** (parallel capacitance) represent the circuit equivalent of a quartz crystal.

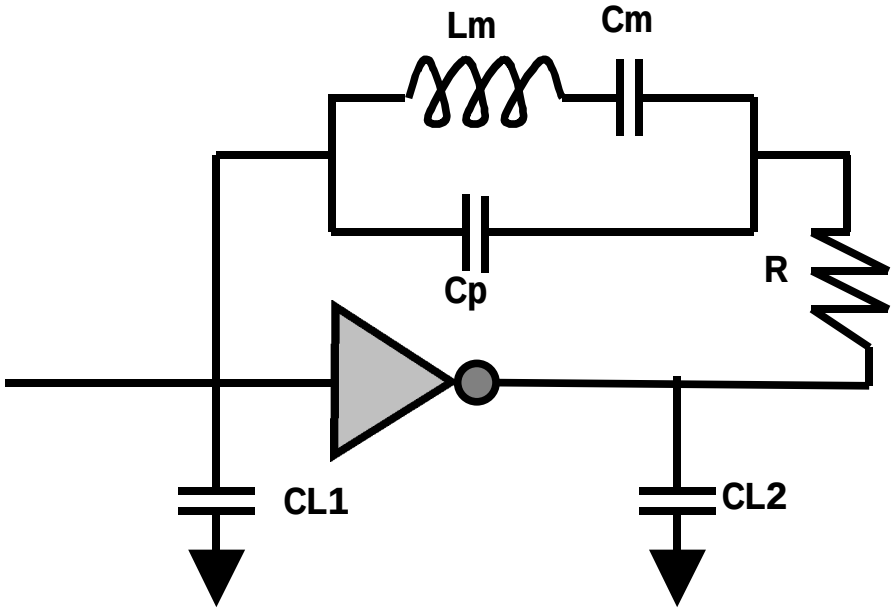


Figure 1 *A Typical Crystal Oscillator Circuit*

Diagnosis: The best way to diagnose this spur is to use a signal generator in place of the crystal. If spur level is impacted, then this is an indication that the oscillator inverter has excessive gain. Note that on some of National Semiconductor's PLLs, the inverting buffer is included on the PLL chip, while on others, it is not. If the power level to the chip is reduced, then this decreases the gain of the buffer, which theoretically should decrease the level of this type of spur.

Cure: In addition to the suggestions about good decoupling and layout, there are several things that may reduce these spur levels

1. Decrease the gain of the inverting buffer

This may sound sort of ridiculous at first, but if the part is run at a lower VCC power supply voltage, then the gain of the inverter is decreased. Also, some of National Semiconductor's PLLs, such as the LMX160x family have only a single inverter stage as opposed to a triple inverter stage.

2. Supply an external inverter

Using a separate inverter for the crystal, or using the inverter from some other component, such as the microprocessor could also be a fix.

3. Increase the value of the Resistor, R

In the above diagram, increasing the value of R can account a little bit for the excessive inverter gain. If R is increased too much, the circuit simply will not oscillate. Note that in many inverter circuits R = 0 Ω.

4. Try unequal load capacitors

Usually, the load capacitors, CL1, and CL2 are chosen to be equal, but in this case it might improve the spur level to make CL2 > CL1. This is because the output of the inverter is a square wave, so anything to round out the edges can help.

5. Layout and filtering

Be sure to read the layout tips and also consider filtering the noisy signal on the board.

Non-Cross talk Related Spurs

These spurs are caused by something other than cross talk on the board. Some common examples are discussed below:

Fractional N Spurs

Description: These spurs only occur with a fractional N PLL. They occur at multiples of the fractional modulus M. For instance, if there was a fractional N PLL with N = 915.2, and a comparison frequency of 1 MHz, there could potentially be spurs at 200 KHz ($1/5^{th}$ fractional spur), 400 KHz ($2/5^{th}$ fractional spur), 600 KHz ($3/5^{th}$ fractional spur), 800 KHz ($4/5^{th}$ fractional spur), and 1 MHz (main spur) from the carrier. If the fraction is N/M, then the k^{th} fractional spur will be present if the greatest common multiple of M and N divide k. For instance, if a PLL is run in the 2/16 mode, spurs will appear at $1/8^{th,}$ $1/4^{th}$, $3/8^{th}$, …, and $7/8^{th}$ of the comparison frequency. Furthermore, the k^{th} fractional spur is most severe when N=k. If N and M are relatively prime, all fractional spurs will be present.

Consider a PLL used in modulo 8 mode. When the fraction is 1/8, all fractional spurs will be present. When the fraction is 2/8, only the even fractional spurs will be present, and the 2/8 fractional spur in this mode will be the worst case for the second fractional spur. When the fraction is 3/8 mode, all fractional spurs will be there and this is the worst case for the third fractional spur. In the 4/8 mode, only the 4/8 and main spur will be present, and this will be the worst case for the fourth fractional spur.

Cause: In any fractional N PLL, fractional N averaging is employed. Fractional N averaging involves switching the N counter value between two different values. This gives rise to fractional spurs due to an instantaneous phase error introduced by the fractional N averaging.

For this reason, compensation circuitry is included on the chip to account for this instantaneous phase error. Since this circuitry is not perfect, there will usually be fractional N spurs on any sort of fractional PLL.

Diagnosis: These spurs are easy to identify because they occur at the fractional modulus times the comparison frequency from the carrier and are very dependent on the fractional modulus.

Cure: Fractional N parts have a lot of part-specific spur causes, but the spurs are all a result of imperfections in the fractional compensation circuitry. They can be dependent on supply voltage, output frequency, and a lot of other attributes that one would normally not suspect. If there is flexibility in adjusting the power supply voltage, then this provides one degree of freedom. For instance, the LMX2350 PLL has lowest fractional spurs around 3.3 V of operation. The other way to deal with these fractional spurs is to use a different fractional N part, since they are specific to each family of fractional N parts. If the second or higher fractional spur is a trouble causer, then using fractional modulus is odd or prime can help, since this will improve the worst case scenario for the second spur.

Greatest Common Multiple Spur

Description: This spur occurs in a dual PLL at the greatest common multiple of the two comparison frequencies. For example, if one side was running with a 25 KHz comparison frequency, and the other side was running with a 30 KHz comparison frequency, then this spur would appear at 5 KHz. In some cases, this spur can be larger on certain output frequencies.

Cause: The reason that this spur occurs is that the greatest common multiple of the two comparison frequencies corresponds to the event that both charge pumps come on at the same time. This result can be derived by considering the periods of the two comparison frequencies. When both charge pumps come on, they produce noise, especially at the charge pump supply pins, which gives birth to this spur.

Diagnosis: A couple telltale signs of this type of spur is it is always spaced the same distance from the carrier, regardless of output frequency. However, keeping the output frequency the same, but changing the comparison frequency causes this spur to move around. Just be sure that when changing the comparison frequencies for diagnostic purposes, you are also changing the greatest common multiple of the two comparison frequencies.

Cure: This spur can be treated effectively by putting more capacitors on the Vcc and charge pump supply lines. Be sure that there is good layout and decoupling around these pins. Also consider changing the comparison frequency of the auxiliary PLL.

Phantom Reference Spur

Description: The phantom reference spur is characterized by a ghastly increase in the reference spurs right after switching frequencies. After the frequency is changed, it takes an excessively long time for the reference spurs to settle down. This spur is more common at lower comparison frequencies.

Cause: Some of this can be possibly explained by deceptive measurements from the equipment, such as using the video averaging function on a spectrum analyzer. It can also be caused by leaky capacitors in the loop filter. Other theories suggest that it is related to undesired effects from the loop filter capacitors, such as dielectric absorption.

Diagnosis: This can be observed on a spectrum analyzer. Just be very careful that it is not some sort of averaging effect of the spectrum analyzer. The output of the spectrum analyzer is power vs. frequency, which is really intended to be a still time sort of measurement. It may be helpful to test the equipment measuring some other spur to make sure that this is really the PLL and not the equipment.

Cure: Designing with higher quality capacitors helps a lot. In particular, the capacitor C2 tends to be the culprit for causing this spur. Common capacitor types listed in order of improving dielectric properties are: tantalum, X7R, NP0, and polypropeline. Also, using a fractional N PLL can possibly help, since the fractional spurs tend to be less leakage dominated.

Prescaler Miscounting Spur

Description: This spur typically occurs at half the comparison frequency. However, it can also occur at one-third, two-thirds, or some fractional multiple of the comparison frequency. It can have mysterious attributes, such only occurring on odd channels.

Cause: This spur is caused by the prescaler miscounting. Things that cause the prescaler to miscount include poor matching to the high frequency input pin, violation of sensitivity specifications for the PLL, and VCO harmonics. Be very aware that although it may seem that the sensitivity requirement for the PLL is being met, poor matching can still agitate sensitivity problems and VCO harmonic problems. Note also that there is an upper sensitivity limitation on the part.

To understand why the prescaler miscounting causes spurs, consider fractional N averaging. Since the prescaler is skipping counts on some occasions and not skipping counts on another, it produces spurs similar to fractional spurs.

Diagnosis: Since miscounting ties in one way or another to sensitivity, try varying the voltage and/or temperature conditions for the PLL. Since sensitivity is dependent on these parameters, any dependency to supply voltage or temperature point to prescaler miscounting as the cause of the spur. Changing the N counter between even and odd values can also sometimes have an impact on this type of spur caused by the N counter miscounting, and can be used as a diagnostic tool.

Also be aware that R counter sensitivity problems can cause this spur as well. One way to diagnose R counter miscounting is to change the R counter value just slightly. If the spur seems sensitive to this, then this may be the cause. If a signal generator is connected to the reference input, and the spur mysteriously disappears, then this suggests that the R counter miscounting is the cause of the spur.

Cure: To cure this problem, it is necessary to fix whatever problem is causing the prescaler to miscount. The first thing to check is that the power level is within the specifications of the part. After that, consider the input impedance of the PLL. For many PLLs, this tends to be capacitive. Putting an inductor to match the imaginary part of the PLL input impedance at the operating frequency can usually fix impedance matching issues. Be also aware of the sensitivity and matching to the VCO harmonics, since they can also cause a miscount. Try to keep the VCO harmonics –20 dBm or lower in order to reduce the chance of the PLL miscounting the VCO harmonic.

VCO Harmonic Spurs

Description: This spur occurs at multiples of the output frequency. All VCOs put out harmonics of some kind. This spur can cause problems if there is very poor matching to the high frequency input of the PLL. Note also in some cases, the higher harmonic can have better matching and sensitivity performance than the fundamental. This can cause mysterious noisy behaviors. In general, it is good to have the second harmonic 20 dB down if possible, but that is very dependent on the matching and the sensitivity of the PLL.

Cause: VCOs are part specific in what level of harmonics they produce, but they all produce undesired harmonics of the fundamental frequency.

Diagnosis: These spurs appear at the VCO frequency and multiples thereof. Change the VCO frequency, and see if the spurs still appear at multiples of the VCO output.

Cure: If the VCO harmonics cause a problem there are several things that can be done to reduce their impact. They can be low pass filtered with LC or RC filters. A resistor or inductor can be placed in series at the fin pin to prevent them from causing the prescaler to miscount. Just make sure that there is good matching and that the spur level at the fin pin is as low as possible. Note also that the many PLLs do not have a 50 Ω input impedance. Treating it as such often creates big problems with the VCO harmonics.

Conclusion

In this chapter some, but not all causes of spurs have been investigated. Although it is difficult to predict the levels of non-reference spurs, their diagnosis and treatment is what is really matters. Non-reference spurs tend to be a thing that requires a lot of hands on type of diagnostics, and process of elimination is sometimes the only way to figure out what is the real cause.

3. Noise Sources in a PLL System

Introduction

This chapter investigates the causes and behaviors of phase noise. The first part gives the theoretical derivations of the noise contributions to the PLL spectra. Whether the user is comfortable with these derivations or not, the second part shows an easy and simple way to apply these concepts to make reasonably accurate estimations of close in phase noise which are accurate to within a few dB most of the time.

PLL Basic Structure

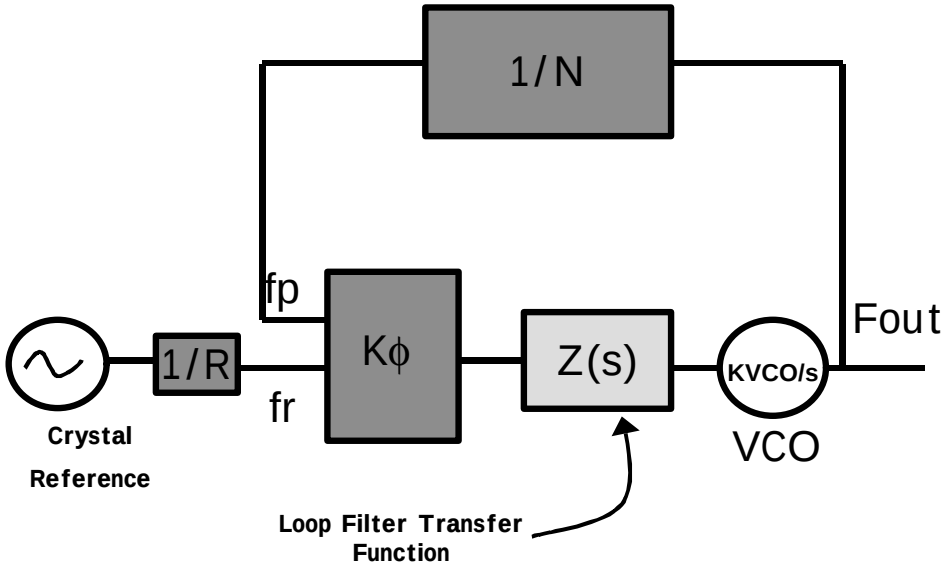


Figure 1 *Basic PLL Structure*

Derivation of Transfer Functions

For the purposes of this chapter calculations are simplified by introducing the following transfer functions:

$$G(s) = \frac{Kf \bullet Kvco \bullet Z(s)}{s} \tag{1}$$

$$H = \frac{1}{N} \tag{2}$$

Using standard control theory, an expression can be written which relates the noise generated at each noise source to the corresponding noise that it produces at the output of the PLL. Table 1 shows various noise sources and the transfer functions that multiply each one.

Source	Transfer Function
Crystal Reference	$\frac{1}{R} \bullet \frac{G(s)}{1+G(s) \bullet H}$
R Divider	$\frac{G(s)}{1+G(s) \bullet H}$
N Divider	$\frac{G(s)}{1+G(s) \bullet H}$
Phase Detector	$\frac{1}{Kf} \bullet \frac{G(s)}{1+G(s) \bullet H}$
Loop Filter Resistor Noise and Active Devices in Loop Filter	See Appendix A and Reference [1]
VCO	$\frac{1}{1+G(s) \bullet H}$

Table 1 *Transfer functions for various noise sources*

Analysis of Transfer Functions

If a noise source is introduced at the source labeled in Table 1, the noise is multiplied by the corresponding transfer function. Note that the crystal noise is multiplied by a factor of $1/R$ and the phase detector is multiplied by a factor of $1/Kf$. It should be apparent that the phase detector noise, N divider noise, R divider noise, and the crystal noise all contain a common factor in their transfer functions. This common factor is given below.

$$\frac{G(s)}{1+G(s) \bullet H} \tag{3}$$

All of these noise sources will be referred to as in-band noise sources. The loop bandwidth, wc, and phase margin, f, are defined as follows:

$$\left\| G(j \bullet wc) \bullet H \right\| = 1 \tag{4}$$

$$180 - \angle G(j \bullet wc) \bullet H = f \tag{5}$$

Using these definitions, equations (1) and (2), and the fact that $G(s)$ is monotonically decreasing in s yields the following:

$$\frac{G(s)}{1+G(s) \bullet H} \approx \begin{cases} N & For w << wc \\ \\ G(s) & For w >> wc \end{cases} \tag{6}$$

However, the VCO noise is multiplied by a different transfer function:

$$\frac{1}{1+G(s) \bullet H} \tag{7}$$

Note that this transfer function (7) can be approximated by:

$$\frac{1}{1+G(s)\bullet H} \approx \begin{cases} \dfrac{N}{G(s)} & For\, w << wc \\ 1 & For\, w >> wc \end{cases} \tag{8}$$

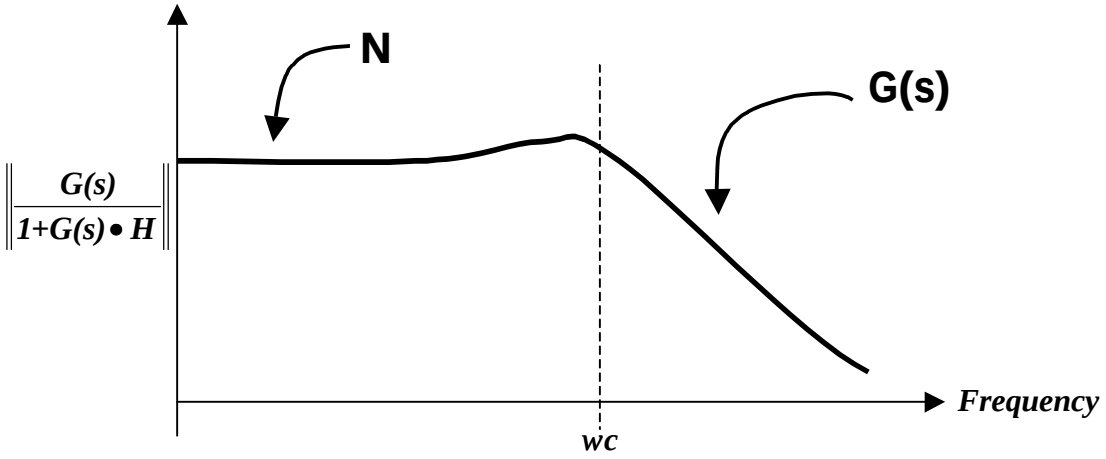


Figure 2 *Transfer Function Multiplying all Noise Sources Except the VCO*

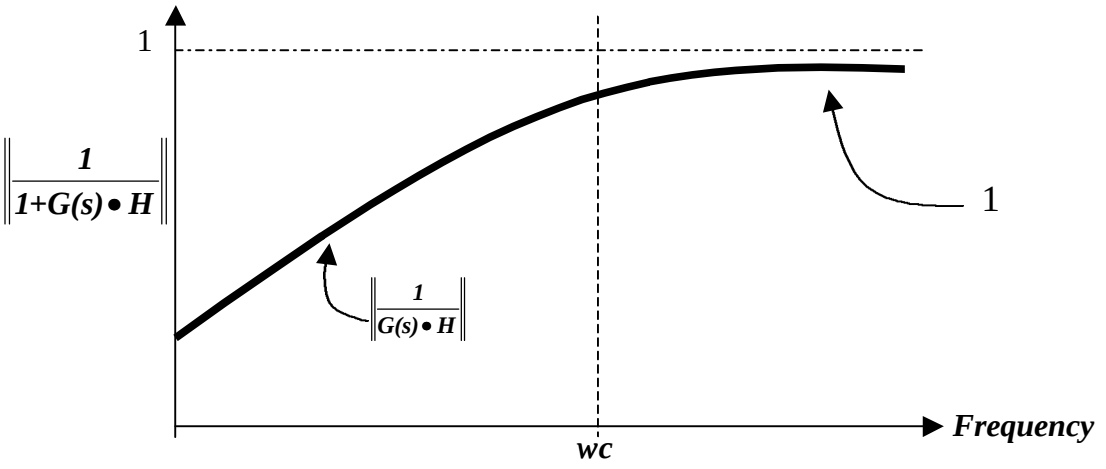


Figure 3 *Transfer Function Multiplying the VCO Noise*

A Few Words About Modulation

The above figures also say something about how to modulate the PLL with information. One way to do this is to modulate the crystal reference. In this case, the loop bandwidth needs to be wider than the information bandwidth of the modulating signal. Another technique is to modulate the VCO voltage. Figure 3 implies that the loop bandwidth needs to be narrow, so the PLL does not track out the modulation. Another technique is to shut down the PLL and keep the VCO running and modulate it this way. By doing this, the PLL does not interfere with the modulated signal, but the frequency will eventually drift away from where it should be and then the PLL needs to be turned on again.

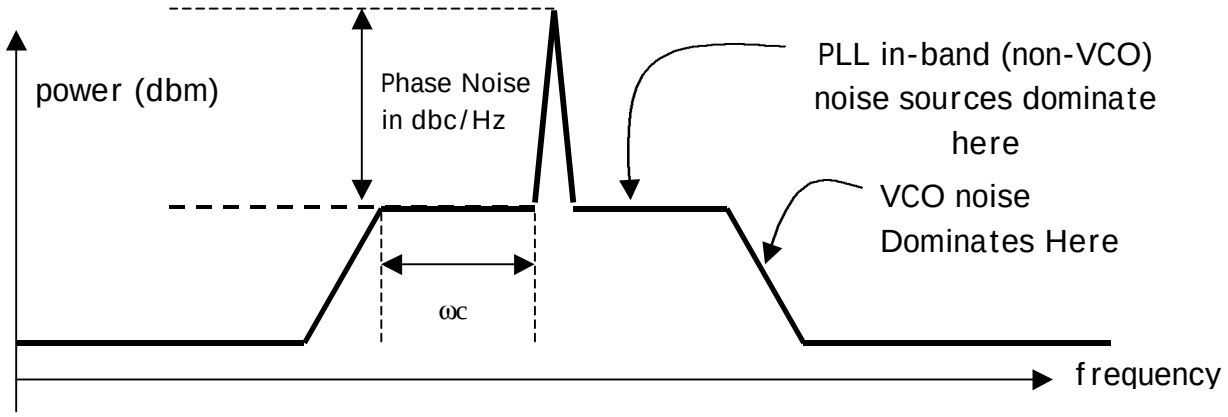


Figure 4 *Typical Phase Noise Spectral Plot for a PLL*

Phase Noise and Phase noise Floor

Although the noise within the loop ($\omega << \omega c$) is dominated by the in-band sources, there may be some slight contribution to this noise from the VCO. This is most noticeable for narrow loop bandwidths, which are less than the theoretical optimal loop bandwidth. However, in cases where the loop bandwidth is at least ten times the phase noise offset frequency, the VCO usually does not contribute significantly to the in-band phase noise.

From the equations in the previous sections, the observation could be made that within the loop bandwidth, the VCO noise contribution should be small, and the in-band noise sources are multiplied by N. Since this is a noise voltage, the noise power would be proportional to N^2, hence the common misconception that the phase noise will vary with ***20•log(N).*** There is nothing wrong with this theory, however, it disregards the effects of the phase detector.

Phase Noise Floor

Phase noise floor is defined as follows:

PhaseNoiseFloor = PhaseNoise (Accounting For Resolution Bandwidth) – 20•log(N) (9)

Noise Contribution Due to the Discrete Sampling Action of the Phase Detector

Assuming a digital 3-state phase-frequency detector, this will put out more noise at higher comparison frequencies. The phase-frequency noise also tends to be the dominant noise source, which is proportional to the comparison frequency. However, the comparison frequency is inversely proportional to N. So the bottom line is that the noise due to the phase detector degrades in accordance with ***10•log(N).***

Prediction of Close in Phase Noise as a Function of N for a Fixed Output Frequency

Combining the ***20•log(N)*** noise improvement due to the transfer function and the ***10•log(N)*** degradation due to the added phase detector noise, the net effect on phase noise is:

10•log(N) (10)

In other words, if N were increased by 10, there would be a 10 dB degradation in the phase noise. This completely describes the variation of phase noise floor in National Semiconductor's AN-1052. This is why phase noise floor is not very meaningful without also knowing the comparison frequency.

Prediction of Close in Phase Noise in General

The phase noise performance is part specific. Table 2 contains typical phase noise data for various National Semiconductor PLLs. It is true that the dividers, Crystal Reference, and VCO contribute to the in-band phase noise, but these are typically dominated by the noise of the phase detector. Since the phase detector noise is dependent on the comparison frequency, this table is normalized for what the phase detector noise would theoretically be for a 1 Hz comparison frequency. This table is based on sample data taken from evaluation boards.

PLL	1 Hz Normalized Phase Detector Noise Floor (dBc/Hz)
LMX233x LMX233xL	-211
LMX23x6 single	-210
LMX15x1,23x5	-206
LMX2350/52	-201@Vcc=3 V, -205 @ Vcc = 5 V
LMX2354	-204
LMX 1600 family	-199

Table 2 *1 Hz Normalized Phase Noise Floor for Various National Semiconductor PLLs*

To predict the close-in phase noise, use:

$$\textit{Phase Noise} = \textit{(1 Hz Normalized Phase Noise Floor from Table)} + 10 \bullet \log(\textit{Comparison Frequency}) + 20 \bullet \log(N) \quad (11)$$

For example, for a 900 MHz VCO with a 200 KHz comparison frequency (N=4500), using an lmx2315, the predicted phase noise would be:

$$-206 + 10 \bullet \log(200000) + 20 \bullet \log(4500) = -80 \ \textit{dBc/Hz} \quad (12)$$

Table 2 gives a rough indication of how one PLL will perform against another. The expected dB difference is simply the difference in the numbers from the table. Note for the fractional N PLL (LMX2350/52), the phase noise floor can be deceptive. Since the fractional N capability allows one to use a higher reference frequency, the actual phase noise tends to be better, despite the fact that the phase noise floor is degraded. This is because the value of N will be smaller. So one should be cautious about comparing the noise floor of this part directly to other parts.

Note that these calculations for phase noise only apply within the loop bandwidth of the PLL. Outside the loop bandwidth, the phase noise is multiplied by the closed loop transfer function, which can be approximated by the spur gain.

Sample Calculation

On the next page, the phase noise is predicted using the LMX2350 PLL and Varil 1960U VCO. This is the data taken from the evaluation board instructions. Note that it is necessary to subtract off ***10•Log(Resolution Bandwidth)*** from the plots of the spectrum analyzer to get the phase noise.

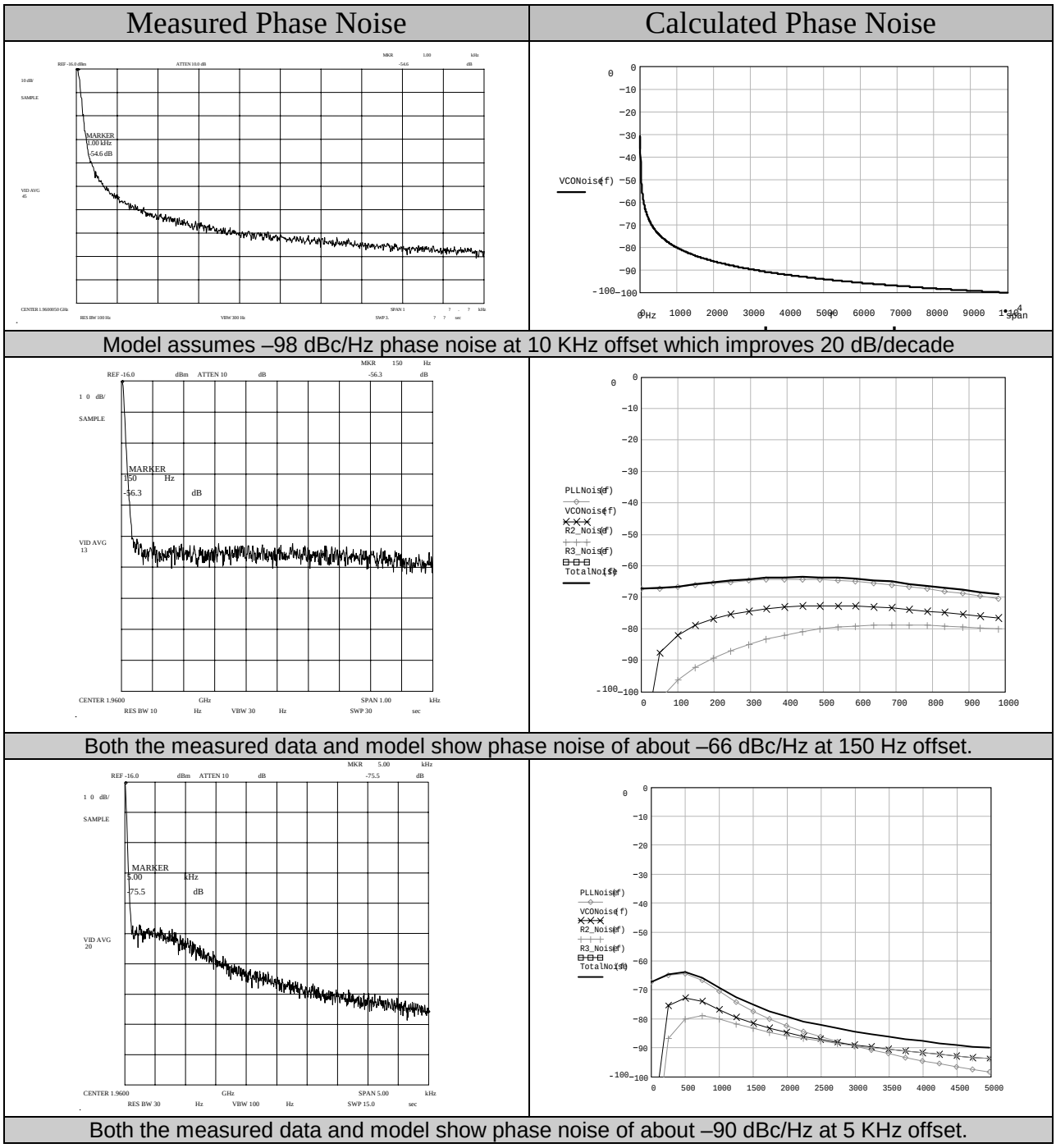


Figure 5 *Measured and Theoretical Phase Noise Example*

Adjustments to the Above Phase Noise Calculations

The phase noise numbers in the table give reasonably accurate estimates for phase noise in most cases. There will be some part to part variation and layout dependency, although these tend to not be very much. The numbers in the chart assume that the in-band phase noise is dominated by the charge pump, which is usually (but not always) the case. There are several other factors that could have an impact on the phase noise.

1. In-Band VCO Phase Noise Contribution

For the purposes of the phase noise calculations presented, the VCO noise contribution within the loop bandwidth is considered to be negligible. Figure 3 indicates that the VCO actually does contribute noise within the loop bandwidth. Within the loop bandwidth, the VCO transfer function is an increasing function with frequency, while the VCO noise is a decreasing function of offset frequency. When these two functions are multiplied together, the result is relatively flat. The VCO tends to contribute more noise within the loop bandwidth in the cases where the loop bandwidth is narrow or in the case of a noisy VCO. For instance, in Figure 5, the VCO noise is contributing about 1 dB to the in-band phase noise.

2. Lower Charge Pump Gain Phase Noise Adjustment

The PLL noise chart assumes that the PLL is in the highest charge pump gain. Note from the transfer functions that the charge pump noise is divided by the charge pump gain. However, it is usually the case that when the charge pump gain is increased, the charge pump noise is increased as well. In some cases, there is no difference in phase noise when the charge pump is used in different gains, and in others, the phase noise is better when the charge pump is used in the higher gains. For this reason, the numbers specified in the table apply to a PLL that is operating with the highest charge pump gain. If this is not the case then the phase noise may be degraded. The influence of the charge pump gain on the phase noise is therefore specific to the PLL chip used. In the case of National Semiconductor parts, a rough rule of thumb is that below 1 mA of charge pump gain, the gain of the charge pump has little effect on the phase noise, but above 1 mA, the charge pump gain does impact the phase noise. Going from a 4 mA to a 1 mA charge pump gain has been measured to cause a typical degradation in phase noise of about 4 dB in the lmx233x family. Going from a 2 mA to a 1 mA mode charge pump gain typically can cause about a 2 dB degradation in the phase noise. This characteristic of having the best phase noise performance at higher charge pump gains is a characteristic of National PLLs along with other manufacturers PLLs as well.

3. Dual PLL Adjustment

In the dual PLL, it has been found that the optimal phase noise performance is when the other side of the PLL is unused, powered down, and with no VCO connected. If this is the case, then this results in a 2 dB improvement from what the table predicts. The table assumes that the other PLL is powered down, but the VCO is connected. If the other side is powered up and running, then the degradation in phase noise may be a dB or two worse than the table predicts. The closer the output frequencies of the two PLLs are, the more severe the phase noise degradation.

4. Noisy Crystal Reference Consideration

It is assumed that the charge pump noise dominates. However, this may not be the case if the crystal reference is noisy. Signal generators, even expensive ones, often increase the phase noise when used as the crystal reference. Spectrum analyzers with a fixed 10 MHz output frequency from the back are usually sufficiently clean enough to use as a crystal reference. The crystal noise is divided by R and multiplied by N. One way to see if a signal generator is too noisy is to double the frequency and double the R value. If the phase noise decreases, then this suggests that the signal generator noise is dominating.

5. Resistor Noise

All resistors create thermal noise. Typically, the contribution from this resistor noise within the loop bandwidth is very negligible. However, this noise contribution can be more significant at farther offsets from the carrier, and even near the loop bandwidth in cases where the resistor, R3, is large. The resistor noise phase noise contribution is decreased if the resistors in the loop filter are decreased. For instance, under the same design parameters, a loop filter that was designed for a higher charge pump current will have lower resistor noise because the calculated values for the resistors will be smaller.

6. Input Sensitivity Violation Problem

There are many ways to cause the phase noise to be worse than predicted. One possible cause of this is when either the VCO or crystal power levels are insufficient to drive the counters. For the high frequency VCO, matching problems can also cause an input sensitivity problem. These phase noise numbers assume that the VCO and crystal power levels are sufficient to drive the counters, and that there are no problems matching the VCO to the prescaler input pin. Although rare, there are also PLLs for which the input buffer contributes phase noise and for these PLLs, a higher crystal oscillator drive level is required for optimal performance.

7. Spectrum Analyzer Correction Factors

A common way of measuring phase noise using a spectrum analyzer is as follows:

Phase Noise = Carrier Power - Noise Power - 10•Log(Resolution Bandwidth)

However, this method is not entirely correct. Spectrum analyzers have a correction factor that is added to the phase noise to account for the log amplifier in the device and minor errors caused due to the difference between the noise bandwidth and 3 dB bandwidth. This correction factor is in the order of about 2 dB. Many spectrum analyzers have a function called "Mark Noise", which does account for the spectrum analyzer correction factors. The part-specific numbers for phase noise derived in this chapter do not account for the correction factor of the spectrum analyzer, and are therefore optimistic by about 2 dB.

Conclusion

This chapter has investigated the causes of phase noise and has provided a somewhat accurate model of how to predict it. Within the loop bandwidth, the PLL phase detector is typically the dominant noise source, and outside the loop bandwidth, the VCO noise is often the dominant noise source. It is reasonable to expect a +- 0.5 dB measurement error when measuring phase noise. Phase noise can vary from board to board and part to part, but typically this variation is in the order of a few dBs.

References

[1] Lascari, Lance *Accurate Phase Noise Prediction in PLL Frequency Synthesizers* Applied Microwave & Wireless Vol.12 No. 5. May 2000

[2] Lascari, Lance *Mathcad PLL Phase Noise Simulation Tool* http://home.rodchester.rr.com/lascari/lancepll.zip

[3] *Phase noise Measurement of PLL Frequency Synthesizers* National Semiconductor Application Note 1052

Appendix A: Basis for 1 Hz Normalized Noise Floor Numbers

Upon reading this chapter, the reader is likely to wonder specifically what is the basis for the 1 Hz Normalized Phase Floor numbers presented in Table 2. It is also likely for the reader to wonder how well these theoretical phase noise numbers compare to measured data. Recall that these numbers were extrapolated from measured data. This data was actually taken from a collection of published information, so that the user can actually go back and find the data that was used to generate this table. There are three sources of published data: evaluation board instructions, characterization reports, and the data book. Evaluation boards provide an excellent source of measured data. The following terminology is used:

PLL -- This is the PLL that was used.

Family -- This is the PLL family. For instance the LMX2330, LMX2331, and LMX2332 are basically the same PLL except for the fact that they have different prescalers. Since parts in the same family have so many similarities, one would expect that their performance in terms of phase noise would be very close.

Fout -- This is the output frequency in MHz

Fcomp -- This is the comparison frequency in KHz

N -- This is the N divider ratio

CP % -- For many PLLs, there are multiple settings for the charge pump current that can be programmed by the user. For some PLLs, this can impact the phase noise. In general, it is best to run the PLL in the highest charge pump gain as possible. The numbers in Table 2 are assuming that the highest charge pump current is used. If this is not the case, then the percentage of maximum charge pump current used is displayed in this column.

CP Adj -- Charge Pump adjustment. In the case where the PLL is not being run in the highest current setting, the expected degradation in phase noise performance (in dB) is displayed in this column. This number is determined by experimentation.

Dual Adj -- In the case of a Dual PLL, it is assumed that the other VCO is running, yet the other PLL is powered off. If the other VCO is actually disconnected, then the phase noise tends to be better by about 2 dB. This modifier in dB is entered in this column

Noise Floor -- This is the 1 Hz Normalized Noise Floor calculated in three ways:

- ***Base*** -- This is the number from Table 2
- ***Adj*** -- This is the base plus any modifiers from CP Adj or Dual Adj
- ***Actual*** -- This is calculated from the actual phase noise measurement

Phase Noise -- This shows the phase noise calculated in two ways:

- ***Predicted*** -- This is calculated using the formulae presented in this chapter
- ***Actual*** This is the actual phase noise measurement.

The phase noise chart is shown on the next page. Note the agreement between the actual and predicted phase noise values. These phase noise numbers do not take into account the correction factors of the spectrum analyzer used to measure them. The reason for this is that this is the way that the phase noise was reported from the actual documents that these numbers were taken from.

Measured Phase Noise for Various National Semiconductor PLLs

Part	Title	Fout	Fcomp	N	CP	CP	Dual	Noise Floor (dBc/Hz)			Phase Noise		
		(MHz)	(KHz)		%	Adj	Adj	Base	Adj	Actual	Predicted	Actual	
Evaluation Boards													
lmx1600	1600eval	1780	200	8900	100	0	0	-199	-199	-197.4981	-67.0019	-65.5	2
lmx1601/02	1601eval	889	200	4445	10	2	0	-199	-197	-197.0677	-71.03226	-71.1	1,2
lmx2306	2306eval	235	50	4700	100	0	0	-210	-210	-210.1317	-89.56834	-89.7	
lmx2316	2316eval	889	200	4445	100	0	0	-210	-210	-207.2677	-84.03226	-81.3	
lmx2326	2326eval	1930	200	9650	100	0	0	-210	-210	-209.7008	-77.29915	-77	
lmx2301	2301eval	137.5	100	1375	100	0	0	-206	-206	-182.2661	-93.23395	-69.5	3
lmx1501	1501eval	900	200	4500	100	0	0	-206	-206	-196.0746	-79.92545	<-70	
lmx1511	1511eval	900	200	4500	100	0	0	-206	-206	-206.0746	-79.92545	-80	
lmx2315	2315eval	900	200	4500	100	0	0	-206	-206	-206.0746	-79.92545	-80	
lmx2325	2325eval	2425	1000	2425	100	0	0	-206	-206	-206.8942	-78.30577	-79.2	
lmx2330	2330aevl	2425	1000	2425	100	0	0	-211	-211	-207.6942	-83.30577	-80	2
lmx2330l	2330levl	2425	1000	2425	100	0	0	-211	-211	-207.2942	-83.30577	-79.6	2
lmx2331	2331evl	1775	200	8875	100	0	0	-211	-211	-211.7737	-79.02633	-79.8	2
lmx2331L	2331levl	1775	200	8875	100	0	0	-211	-211	-211.7737	-79.02633	-79.8	2
lmx2332	2332aevl	900	200	4500	100	0	0	-211	-211	-207.0746	-84.92545	-81	2
lmx2332L	2332leval	900	200	4500	100	0	0	-211	-211	-207.0746	-84.92545	-81	2
lmx2336	2336eval	1830	200	9150	25	4	0	-211	-207	-207.0387	-74.76128	-74.8	2
lmx2336	2336evla	1780	200	8900	100	0	0	-211	-211	-210.6981	-79.0019	-78.7	2
lmx2350	2350eval	1960	160	12250	100	0	0	-201	-201	-200.2039	-67.19608	-66.4	2
lmx2352	2352eval	902	160	5638	100	0	0	-201	-201	-200.2629	-73.93707	-73.2	2
Characterization Data													
lmx2331A	LowPwr	1653	300	5510	100	0	-2	-211	-213	-213.0942	-83.40576	-83.5	2
lmx2331L	LowPwr	1653	300	5510	100	0	-2	-211	-213	-212.8942	-83.40576	-83.3	2
lmx2332A	LowPwr	1017	25	40680	100	0	-2	-211	-213	-211.767	-76.83298	-75.6	2
lmx2332L	LowPwr	1017	25	40680	100	0	-2	-211	-213	-211.467	-76.83298	-75.3	2
lmx1600	LowCost	903	25	36120	100	0	-2	-199	-201	-199.3344	-65.86565	-64.2	2
lmx1600	LowCost	903	200	4515	100	0	-2	-199	-201	-200.8035	-74.89654	-74.7	2
lmx1601	LowCost	903	25	36120	100	0	-2	-199	-201	-199.1344	-65.86565	-64	2
lmx1601	LowCost	903	200	4515	100	0	-2	-199	-201	-200.6035	-74.89654	-74.5	2
lmx1602	LowCost	903	25	36120	100	0	-2	-199	-201	-199.5344	-65.86565	-64.4	2
lmx1602	LowCost	903	200	4515	100	0	-2	-199	-201	-200.4035	-74.89654	-74.3	2
lmx2306	LowPwr	235	50	4700	100	0	0	-210	-210	-207.2317	-89.56834	-86.8	
lmx2306	LowPwr	245	50	4900	100	0	0	-210	-210	-202.7936	-89.20638	-82	
lmx2306	LowPwr	250	50	5000	100	0	0	-210	-210	-208.4691	-89.0309	-87.5	
lmx2316	LowPwr	889	200	4445	100	0	0	-210	-210	-207.2677	-84.03226	-81.3	
lmx2316	LowPwr	902	200	4510	100	0	0	-210	-210	-206.7938	-83.90617	-80.7	
lmx2316	LowPwr	915	200	4575	100	0	0	-210	-210	-207.9181	-83.78188	-81.7	
Databook													
lmx1511	DataSheet	886	25	35440	100	0	0	-206	-206	-210.4693	-71.03073	-75.5	
lmx2320	DataSheet	1669	300	5563	100	0	0	-206	-206	-210.7779	-76.32209	-81.1	
lmx2315	AN-1001	900	200	4500	100	0	0	-206	-206	-205.6746	-79.92545	-79.6	
lmx2332A	AN-1052	900	31.25	28800	100	0	-2	-211	-213	-213.9363	-78.86365	-79.8	2
Comments													
1. For the LMX233x, 4X current mode is 4 dB better than 1X.													
2. Best performance is with IF VCO disconnected, 2nd best with IF poweroff, 3rd IF running.													
3. These boards have discrete VCOs and narrow loop bandwidths, thus their bad in-band phase noise.													

Appendix B: Phase Noise for Resistors and Active Devices

Noise Voltages

Resistors and active devices such as op-amps generate noise voltages. In the case of an op-amp, the noise voltage should be specified. In the case of a resistor, this noise voltage is the thermal noise generated by the resistor. Recall that the thermal noise generated by a resistor is:

$$R\_Noise = \sqrt{4 \bullet T_0 \bullet K \bullet R}$$

T_0	=	Ambient Temperature in Kelvin	=	300 Kelvin (typically)
K	=	Boltzman's Constant	=	1.380658×10^{-23} (Joule/Kelvin)
R	=	Resistor Value in ohms		

Note that in both the case of the resistor and op-amp, the units are $\frac{V}{\sqrt{Hz}}$. Since phase noise is normalized to a 1 Hz bandwidth, one can disregard the denominator and consider the units to be in Volts.

Transfer Function for the Noise Voltage

Once the noise voltage is known, an open-loop transfer function, T(s), can be written which relates this noise voltage to the voltage it would generate for an open loop system at the VCO tuning line. To account for the closed loop system, one can simply divide this by the open loop transfer function of the VCO[1]. In deriving the transfer function, T(s), it is simplifies calculations if one remembers that all the grounds are connected and draws a short between them. In the case of a resistor noise transfer function, the resistor noise can be considered to be acting on either side of the resistor. The actual transfer functions will not be derived here, since the formulas are shown in the design example at the end of this chapter.

Translating the Noise Voltage to a dBc/Hz number for Phase Noise

This explanation is found in reference [1]. In a similar way that leakage-based reference spur was shown to relate to the modulation index of the signal, the modulation index is applied here to derive the phase noise. Vnoise represents the noise voltage that would be generated at the VCO input for an open loop system, f is the frequency, and G is the open loop transfer function. Note that it is necessary to multiply the noise voltage by a factor of $\sqrt{2}$, since these are expressed as RMS, and not Peak to Peak.

$$Phase\ Noise \approx 20 \bullet \log\left(\frac{b}{2}\right) \qquad For\ b << 1$$

$$b = \frac{\sqrt{2} \bullet Vnoise \bullet Kvco}{f} \bullet \frac{\left|T(2 \bullet p \bullet i \bullet f)\right|}{\left|1 + \frac{G(2 \bullet p \bullet i \bullet f)}{N}\right|}$$

Resistor noise becomes a problem when the resistors in the loop filter get too large. The resistor noise tends to have the greatest contribution at frequencies close to the loop bandwidth. It can also have some contribution outside the loop bandwidth. Using a higher current gain or Fractional N PLL can reduce the impact of resistor noise. Op-amp noise can also add considerable phase noise, especially if the op-amp is not very low noise.

PHASE NOISE ANALYSIS

ENTER PARAMETERS HERE

$K\phi := 5 \cdot mA$ $Fcomp := 1000 kHz$ $Fout := 900 MHz$ $Kvco := 20 \frac{MHz}{volt}$

$C1 := 4.259 nF$ $C2 := 75.15 nF$ $C3 := 852 pF$ $C4 := 106 pF$

$R2 := 0.582 k\Omega$ $R3 := 1.814 k\Omega$ $R4 := 1.814 k\Omega$

CALCULATE PARAMETERS

$N := \frac{Fout}{Fcomp}$ $N = 900$

$a := R2 \cdot R3 \cdot R4 \cdot C1 \cdot C2 \cdot C3 \cdot C4$ $d := C1 + C2 + C3 + C4$

$b := C1 \cdot C2 \cdot R2 \cdot R3 \cdot (C3 + C4) + R4 \cdot C4 \cdot (C2 \cdot C3 \cdot R3 + C1 \cdot C3 \cdot R3 + C1 \cdot C2 \cdot R2)$

$c := R2 \cdot C2 \cdot (C1 + C3 + C4) + R3 \cdot (C1 + C2) \cdot (C3 + C4) + R4 \cdot C4 \cdot (C1 + C2 + C3)$

$Z(s) := \frac{1 + R2 \cdot C2 \cdot s}{s \cdot (a \cdot s^3 + b \cdot s^2 + c \cdot s + d)}$ Loop Filter Impedanc

$G(s) := \frac{K\phi \cdot Kvco \cdot Z(s)}{s}$ Forward Loop Gain

$CL(s) := \frac{G(s)}{1 + \frac{G(s)}{N}}$ Closed Loop Gain

BANDWIDTH AND PHASE MARGIN

$x := 1.0 kHz$

$Fc := root(|G(x \cdot 2 \cdot \pi \cdot i)| - N, x)$ $Fc = 9.989 kHz$ Loop Bandwidth

$f := Fc$

$arg(G(Fc \cdot 2 \cdot \pi \cdot i)) \cdot \frac{180}{\pi} + 180 = 53.098$ Phase Margin

PHASE NOISE PROFILE

$Noise1Hz := -213$ dbc/Hz

1 Hz Normalized Phase Detector Noise
LMX2330, Aux side powered down,
High charge pump gain setting

$$NoiseFloor := Noise1Hz + 10\log\left(\frac{Fcomp}{Hz}\right)$$

$NoiseFloor = -153$ dbc/Hz

Phase Noise Floor

$$PLLNoise(f) := NoiseFloor + 20\log\left(\left| CL(f \cdot 2 \cdot \pi \cdot i) \right|\right)$$

$PLLNoise(150Hz) = -93.91$

Close In Phase Noise

VCO Noise

Assumes that the VCO Noise changes 20 db/decade

$VCO10khz := -100$ dbc/Hz

$$VCONoise(f) := VCO10khz - 20\log\left(\frac{f}{10kHz}\right) - 20\log\left(\left| 1 + \frac{G(f \cdot 2 \cdot \pi \cdot i)}{N} \right|\right)$$

Resistor Noise Properties

$k := 1.380650 \cdot 10^{-23} \cdot \frac{joule}{K}$ $T_o := 300K$ $R\_Noise(R) := \sqrt{4 \cdot T_o \cdot k \cdot R \cdot 1Hz}$

R2 Resistor Noise

$VnR2 := R\_Noise(R2)$ $VnR2 = 3.105 \cdot 10^{-9}$ volt

$$Z1(s) := \frac{1}{s \cdot C2} + R2$$

$$Z(s) := \frac{1}{s \cdot (C1 + C3 + C4 + s \cdot (C3 \cdot C4 \cdot R4 + C3 \cdot R3 \cdot C1 + C4 \cdot R4 \cdot C1 + R3 \cdot C4 \cdot C1) + s^2 \cdot C1 \cdot C3 \cdot C4 \cdot R3 \cdot R4)}$$

$$TR2(s) := \left| \frac{1}{1 + \frac{G(s)}{N}} \cdot \frac{Z1(s)}{Z1(s) + Z(s)} \right|$$

$$R2\_Noise(f) := 20\log\left(\left| \frac{\sqrt{2} \cdot VnR2 \cdot TR2(2 \cdot \pi \cdot i \cdot f) \cdot Kvco}{2 \cdot f} \right|\right)$$

R3 Resistor Noise

$VnR3 := R\_Noise(R3)$ $VnR3 = 5.482 \cdot 10^{-9} \cdot volt$

$$Z1(s) := \frac{1 + s \cdot C2 \cdot R2}{s \cdot (C1 + C2) + s^2 \cdot C1 \cdot C2 \cdot R2} + R3 \qquad Z2(s) := \frac{1 + s \cdot C4 \cdot R4}{s \cdot C3 + s \cdot C4 + s^2 \cdot C3 \cdot C4 \cdot R4}$$

$$TR3(s) := \frac{1}{\left| 1 + \frac{G(s)}{N} \right|} \cdot \left| \frac{Z1(s)}{Z1(s) + Z2(s)} \cdot \frac{1}{1 + s \cdot C4 \cdot R4} \right|$$

$$R3\_Noise(f) := if\left(R3 > 1 \cdot \Omega , 20 \log\left(\left| \frac{\sqrt{2} \cdot VnR3 \cdot TR3(2 \cdot \pi \cdot i \cdot f) \cdot Kvco}{2 \cdot f} \right| \right), -500 \right)$$

R4 Resistor Noise

$VnR4 := R\_Noise(R3)$ $VnR4 = 5.482 \cdot 10^{-9} \cdot volt$

$$Z2(s) := \frac{1 + s \cdot C2 \cdot R2}{s \cdot (C1 + C2) + s^2 \cdot C1 \cdot C2 \cdot R2} \qquad Z(s) := R4 + \frac{R3 + Z2(s)}{1 + s \cdot C3 \cdot R3 + s \cdot C3 \cdot Z2(s)}$$

$$TR4(s) := \frac{1}{\left| 1 + \frac{G(s)}{N} \right|} \cdot \left| \frac{1}{1 + s \cdot C4 \cdot Z(s)} \right|$$

$$R4\_Noise(f) := if\left(R4 > 1 \cdot \Omega , 20 \log\left(\left| \frac{\sqrt{2} \cdot VnR4 \cdot TR4(2 \cdot \pi \cdot i \cdot f) \cdot Kvco}{2 \cdot f} \right| \right), -500 \right)$$

Reference Spurs

$BaseLeakageSpur := 16.0$ dbc — This is a universal empirical constant

$LeakageCurrent := 10^{-9} \cdot amp$ — Enter the leakage current of the PLL

$BasePulseSpur := -311$ dbc — This is a part-specific constant

Calculations

$SpurGain := 20 \log(|G(Fcomp)|)$ $SpurGain = 13.924$

$$LeakageSpur := BaseLeakageSpur + 20 \log\left(\frac{LeakageCurrent}{K\phi} \right) + SpurGain$$

$$PulseSpur := BasePulseSpur + SpurGain + 40 \log\left(\frac{Fcomp}{1 \cdot Hz} \right)$$

$$TotalSpur(f) := if\left(|f - Fcomp| < 1000 \cdot Hz , 10 \log\left(10^{\frac{PulseSpur}{10}} + 10^{\frac{LeakageSpur}{10}} \right), -500 \right)$$

$LeakageSpur = -104.055$ $PulseSpur = -57.076$ $TotalSpur(Fcomp) = -57.076$

Total Noise Properties

$$TotalNoise(f) := 10\log\left(10^{\frac{PLLNoise(f)}{10}} + 10^{\frac{VCONoise(f)}{10}} + 10^{\frac{R2\_Noise(f)}{10}} + 10^{\frac{R3\_Noise(f)}{10}} + 10^{\frac{R4\_Noise(f)}{10}} + 10^{\frac{TotalSpur(f)}{10}}\right)$$

$$10^{\frac{VCO10kHzNoiseFloor - 20\log(N)}{20}} \cdot 10kHz = 4.968kHz$$ Min RMS Bandwidth

$$\sqrt{\sec \cdot \int_{100Hz}^{50kHz} 10^{\frac{TotalNoise(f)}{10}}\, d\omega} = 0.21deg$$ RMS Phase Error

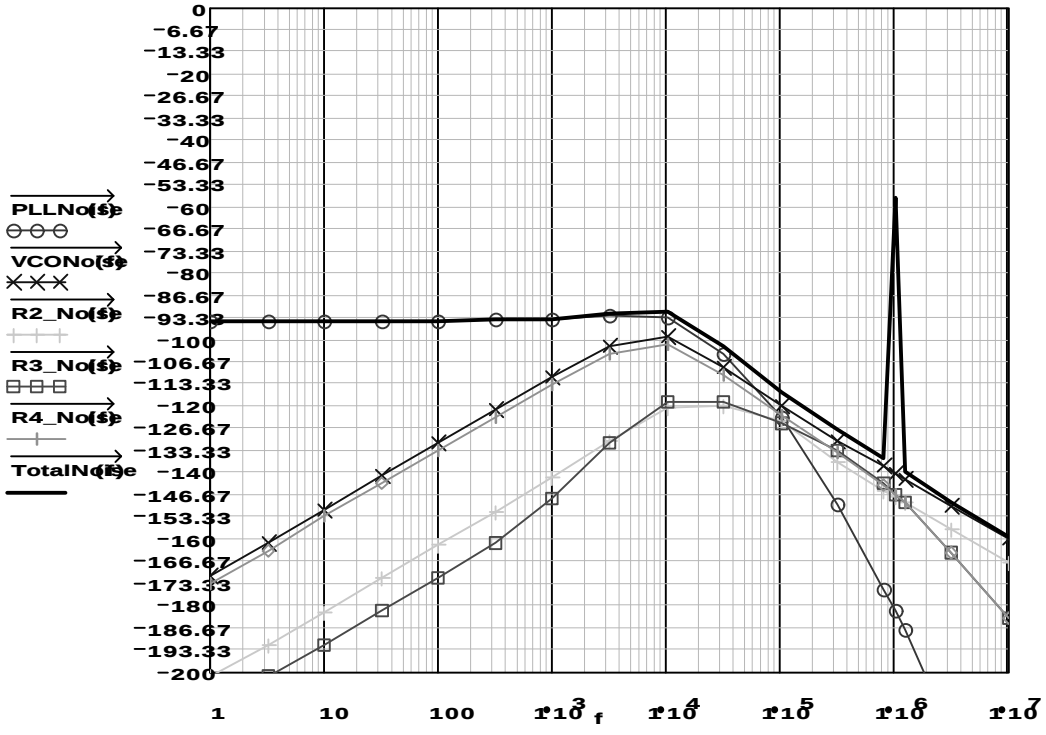
Simulated Spectrum Analyzer

$span := 10Fcomp$ Enter the Span in kHz

Phase Noise/Spurs at Various Offsets

$TotalNoise(100Hz) = -93.911$ dbc/Hz Close-in Phase Noise

$TotalNoise(Fcomp) = -57.076$ dbc First Reference Spur (Worst Case)



Note that the factor of 180/π is not used in the calculation for the RMS phase error. The reason for this is that mathcad automatically converts this number from radians to degrees, and therefore, this conversion factor is not necessary. RMS phase error is discussed in the next chapter.

4. RMS Phase Error and Signal to Noise Ratio

Introduction

This chapter discusses RMS Phase error, how to calculate it, the relevance it has in digital communications, and how to minimize it. It also discusses the signal to noise ratio of a PLL and it's relationship to phase noise.

What is RMS Phase Error?

There are three different ways of visualizing RMS phase error. It can be visualized in the time domain, in the frequency domain, or in a constellation diagram. These different interpretations of RMS phase error are all related and discussed below.

RMS Phase Error In the Time Domain

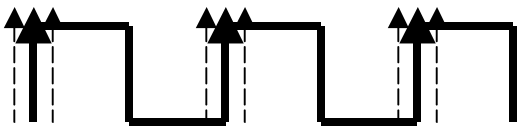


Figure 1 *Illustration of RMS Phase Error of a Signal in the Time Domain*

The above figure shows a square wave Note that the rising edges of the square wave do not always occur at exactly the time they should, but have a random phase error that can be either positive or negative. Now the average value of this phase error is zero, but the standard deviation is nonzero and is called the RMS phase error. Recall for the normal distribution, approximately 68% of the area of the normal distribution curve is within one standard deviation of the mean. This means that if one was to take a random sample of the starting phase, 68 % of the time it would be within the RMS phase error. Notice how the rising edges of the signal do not always start at the time they should, but sort of jitters. For this reason, RMS phase error and phase noise are often referred to as "phase jitter". Although the output of a PLL tends to be a sine wave (instead of a square wave), there is little loss of generality here, because the sine wave goes through counters that turn it into a square wave.

For an example, consider a 10 MHz signal with 5 degrees RMS phase error. Since the period of this signal is 0.1 uS, a 5 degree RMS phase error imply a normally distributed random phase shift which has a standard deviation of 1.339 nS.

RMS Phase Error Calculation from Frequency Domain

Formula for Relating Spectral Density to RMS Phase Error

RMS Noise is calculated by integrating the phase noise, taking the square root, and then converting this number from radians to degrees. The limit, ***a***, tends to be very close to the carrier, and the limit, ***b***, tends to be much farther away, typically outside the loop bandwidth. Assuming ***b*** to be infinite gives a reasonable approximation to RMS phase error. The RMS phase error in degrees is calculated as:

$$RMS\ Phase\ Error = \frac{180}{p} \bullet \sqrt{2 \bullet \int_a^b L(f) \bullet df} \qquad (1)$$

Derivation of RMS Phase Error Formula

The derivation for formula (1) will now be given. Recall that phase noise is measured in dBc/Hz on a spectrum analyzer, which shows the output power vs. frequency. Since phase noise is measured at a particular frequency output, it can be thought of as the ratio of the carrier frequency power to the noise power, expressed in a decibel scale. Actually, it is more correct to view this as a phase noise density, even though it is commonly just referred to as phase noise. To obtain the total phase error, the phase noise (density) is integrated over the whole frequency spectrum. The factor of two is there to account for the phase noise on both sides of the carrier.

Since the spectrum analyzer displays power vs. frequency, and not voltage vs. frequency, it is necessary to take the square root of the integrated product to obtain an RMS (Root Mean Square) error. Recall that in statistics, the standard deviation of a continuous random variable is obtained by integrating the square of the probability distribution function and then applying the square root. An analogous procedure is used in the calculation of RMS phase error and this is why the RMS phase error relates to the standard deviation of the phase error. Since the number obtained is a dimensionless value in radians, it is necessary to convert this to degrees.

Approximate RMS Phase Error Calculation

To calculate the RMS noise correctly, the spectral density needs to be known. However, it is sometimes convenient to use a rule of thumb to simplify calculations, or in situations where the VCO noise is unknown. One good rule of thumb is to assume that the phase noise decreases 20 dB/decade from the PLL loop bandwidth. This approximation is shown in Figure 2.

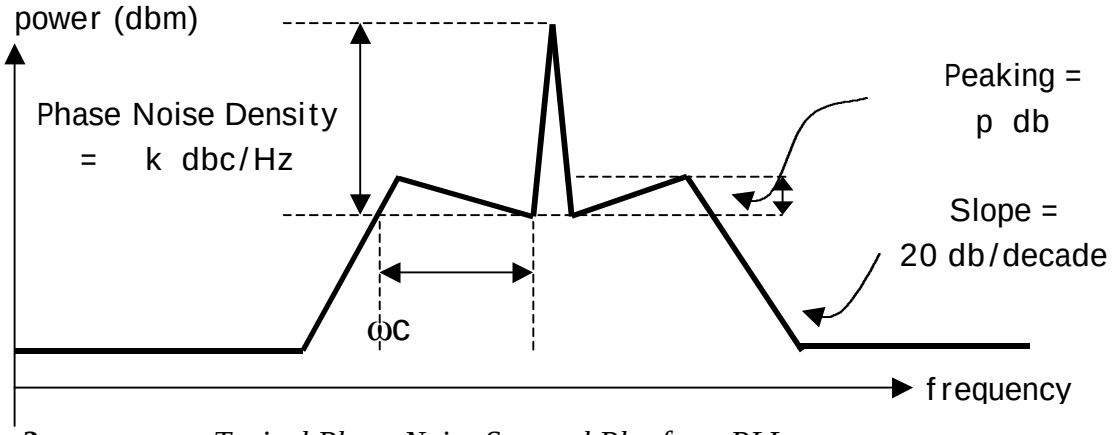


Figure 2 *Typical Phase Noise Spectral Plot for a PLL*

Approximate Calculation of RMS Phase Error

To calculate the RMS Phase Error, formula (1) will now be applied. Since the phase noise density, k, is expressed in dBc/Hz, it is necessary to convert this from decibels to scalar units before the integration is performed.

$$RMSnoise = \frac{180}{p}\sqrt{2 \bullet \left(\int_0^{fc} 10^{k/10} \bullet \left(1 + \left[10^{p/10} - 1\right] \bullet \frac{f}{fc}\right) \bullet df + \int_{fc}^{\infty} 10^{(k+p)/10 - 20 \bullet \frac{\log(f - fc + 1)}{10}} \bullet df \right)}$$

$$= \frac{180}{p} \bullet 10^{k/20} \sqrt{fc \bullet \left(1 + 10^{p/10}\right) + 10^{p/10} \bullet 2}$$

Note that for the purposes of simplifying calculations, it was assumed that the phase noise peaks at the loop bandwidth, but in actuality, the peaking occurs slightly before the loop bandwidth as shown in Figure 2. This causes these estimations to be slightly lower than they actually should be. Three dB is a typical value for the peaking, which would be typical for 45 degrees of phase margin, however, it makes sense to use a value slightly higher, since this will help compensate for the fact that the estimates are slightly low. A good value of peaking to use is 4 dB. For the sake of simplicity, it makes sense to introduce approximations. Note that the second term under the square root is very small compared to the first term for any loop bandwidth that is reasonable. If one neglects the second term and assumes 4 dB of peaking, the formula can be greatly simplified.

$$RMSnoise = 107 \bullet 10^{k/20} \sqrt{fc}$$

If 0 dB of peaking, then multiply this result by 75%. If 3 dB of peaking is assumed, then multiply this result by 92%. If 10 dB of peaking is assumed, multiply this result by 177%.
For a System with 10 KHz loop bandwidth, and –80 dBc/Hz phase noise, (assume 4dB peaking):

$$RMS\ Phase\ Error = 107 \bullet 10^{-80/20} \bullet \sqrt{10000} = 1.1^{o}$$

Choice of Loop Bandwidth for Optimal RMS Phase Error

This formula implies that a PLL with a narrower loop bandwidth will have less RMS phase error, but in fact this is only true to a point. The validity of the approximations used in the above formula degrades if the loop bandwidth is too narrow. After decreasing the loop bandwidth beyond this point (where the PLL noise equals the VCO noise), the phase error actually starts to increase. It follows that for optimal RMS phase error, one should choose the loop bandwidth of the system such that the PLL noise is equal to the free-running VCO noise at that point. This is because within the loop bandwidth, the main noise contribution is from the PLL (everything except for the VCO), while outside of the loop bandwidth, the main noise contribution is the VCO. This optimal loop bandwidth is typically a few kilohertz.

RMS Phase Error Interpretation in the Constellation Diagram

If one visualizes the RMS error in the time domain, then it can be seen why this may be relevant in clock recovery applications, or any application where the rising (or falling) edges of the signal need to occur in a predictable fashion. The impact of RMS phase error is more obvious when considering a constellation diagram.

The constellation diagram shows the relative phases of the I (in phase) and Q (in quadrature – 90 degrees phase shift) signals. The I and Q axes are considered to be orthogonal, since their inner product is zero. In other words, for any signal received, the I and Q component can be recovered. Each point on the constellation diagram corresponds to a different symbol, which could represent multiple bits. As the number of symbols is increased, the bandwidth efficiency theoretically increases, but the system also becomes more susceptible to noise. Quadrature Phase Shift Keying (QPSK) is a modulation scheme sometimes used in cellular phones. Figure 3 shows the constellation diagram for QPSK.

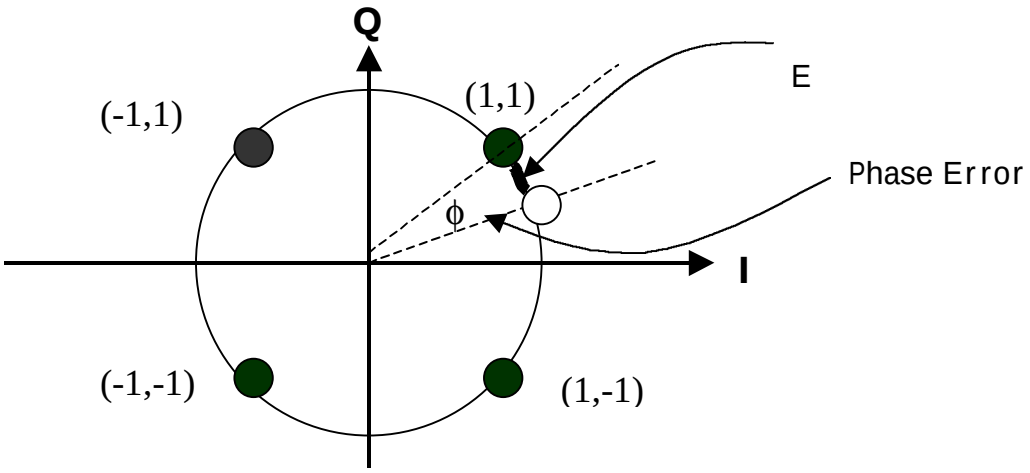


Figure 3 *Impact of RMS phase Error Seen on a Constellation Diagram*

Consider an ideal system in which the only noise-producing component is the PLL in the receiver. In this example, the symbol corresponding to the bits (1,1) is the intended message indicated by the darkened circle. However, because the PLL has a non-zero RMS phase error contribution, the received signal is actually the non-filled circle. If this experiment was repeated, then it the result would be that the phase error between the received and intended signal was normally distributed with a standard deviation equal to the RMS phase error. If the RMS phase error of the system becomes too large, it could actually cause a the message to be misinterpreted as (-1, 1) or (1,-1). This constellation diagram interpretation of RMS phase error shows why higher order modulation schemes are more subject to the RMS phase error of the PLL. A real communications system will have a noisy channel and other noisy components, which reduce the amount of RMS phase error of the PLL that can be tolerated.

Other Interpretations of RMS Phase Error

Eye Diagram

One popular way of viewing RMS phase error is the eye diagram. The impact of the RMS phase error on the eye diagram is that it causes it to close up. This means that the decision region is smaller and it is more likely to make an error in which bits were sent.

Error Vector Magnitude (EVM)

Error Vector Magnitude is the magnitude of the vector formed from the intended message and the actual message received (refer to Figure 3). This is commonly expressed as a percentage of the error vector relative to the vector formed between the origin and intended message. Referring to Figure 3, assuming the circle has radius R, and applying the law of cosines yields the magnitude of the error vector , ***E***, to be:

$$E = 2 \bullet R^2 - 2 \bullet R^2 \bullet \cos(f)$$

Assuming that ϕ is small, and using the Taylor series expansion $\cos(\phi) = 1 - \phi^2/2$, yields the following relationship between RMS phase error and EVM:

$$EVM \approx 100\% \bullet \left(\frac{p}{180} \right) \bullet (RMS \ \ Phase \ \ Error \ \ in \ \ Degrees)$$

Signal to Noise Ratio (SNR)

The signal to noise ratio of a PLL refers to the carrier power to the noise power. Since phase noise is expressed in terms of dBc/Hz. Without loss of generality, the signal can be considered to be concentrated in a 1 Hz bandwidth with relative power level of 0 dBc/Hz. The total power for this signal is 0 dBc.

The noise power can be found by integrating the power spectral density, except for the carrier. The lower integration limit, ***a***, can be assumed to be 0 Hz, just as long as the carrier is disregarded. The upper integration limit, ***b***, is the bandwidth of interest, perhaps the channel spacing. Choosing ***b*** to be infinite typically serves as a reasonable approximation for general purpose discussions. The signal to noise ratio in dB is therefore:

$$SNR = \frac{1}{2 \bullet \int_0^b L(f) \bullet df}$$

There are other ways to define the signal to noise ratio of a PLL as well. To correctly figure how the SNR of a PLL impacts the SNR of a system is actually a detailed calculation. However, a simple analogy can be used to give a rough idea of how the PLL SNR impacts the system.

Consider an input signal to a mixer:

$$S1 = Si + Ni$$

Where S1 is the total input signal, Si is the desired input signal, and Ni is the undesired input noise. Now assume that the PLL signal is:

$$S2 = Spll + Npll$$

The output signal is therefore the product of the two signals S1 and S2

$$Sout = Spll \bullet Si + Spll \bullet Ni + Si \bullet Npll + Npll \bullet Ni$$

Now the first term is the desired signal power and the last term is negligible. The output signal to noise ratio can therefore be approximated as:

$$SNR = \frac{Spll \bullet Si}{Spll \bullet Ni + Si \bullet Npll} = \frac{SNR1 \bullet SNR2}{SNR1 + SNR2}$$

In the above equation, ***SNR1*** and ***SNR2*** represent the signal to noise ratios of ***S1*** and ***S2***, respectively. In an analogous way that two resistances combine in parallel, the lower signal to noise ratio dominates. The above calculations contain some very gross approximations, but they do show how the signal to noise ratio of the PLL can degrade the signal to noise ratio of the whole system.

Conclusion

This chapter has covered various parameters that are derived from the phase noise of the PLL, including RMS phase error. Unlike the phase noise discussed in the previous chapter, the RMS phase error is very dependent on the loop bandwidth of the PLL. RMS phase error is often a parameter of concern in digital communication systems, especially those using phase modulation.

5. Transient Response of PLL Frequency Synthesizers

Introduction

This chapter considers the frequency response of a PLL when the N divider is changed. In addition to giving a fourth order model of this event, whose only approximation is the continuous time approximation for the phase detector, it also gives derivations for natural frequency and damping factor, which are used in a second order approximation. It further relates them to loop bandwidth and phase margin. This chapter is intended to give a rigorous mathematical foundation for the transient response of PLL synthesizers. In doing so, it provides a universal model which can be used in place of all of the various rules of thumb, since rules of thumb only work under certain conditions or for certain applications.

PLL Basic Structure

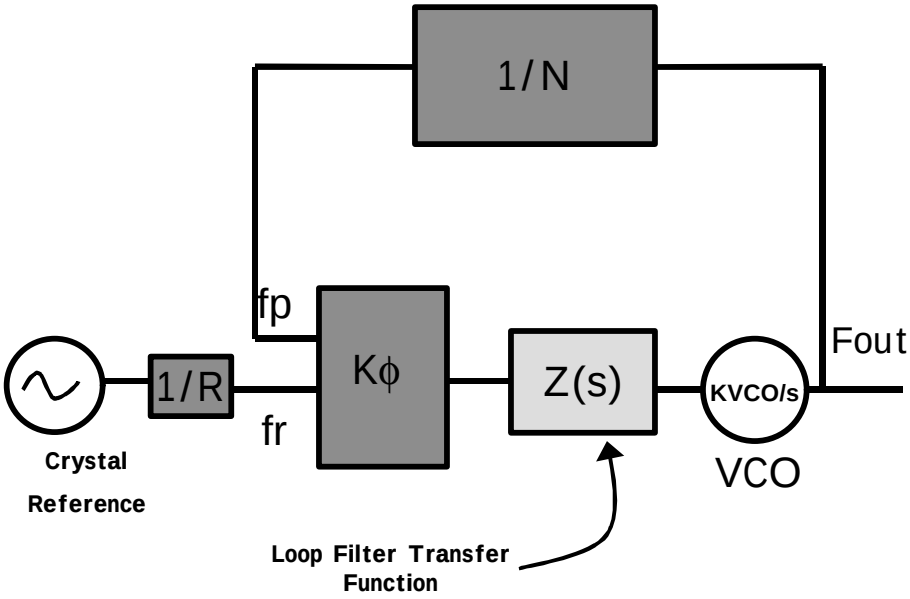


Figure 1 *Basic PLL Structure*

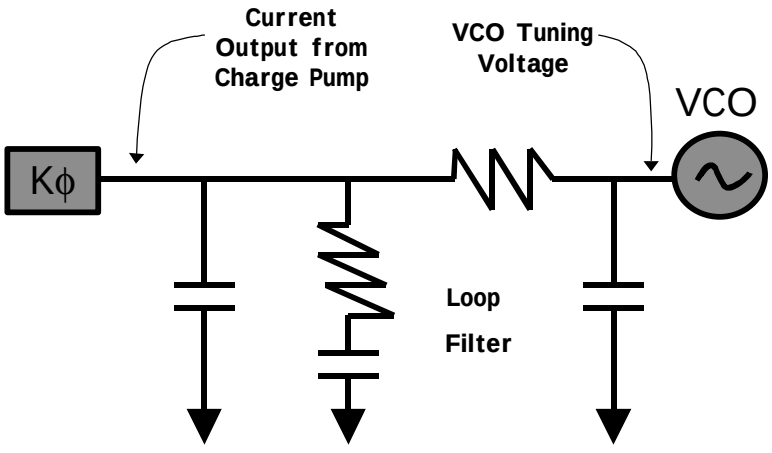


Figure 2 *Assumed Passive Third Order Loop Filter Topology*

Derivation of Transfer Functions

Define the following constants:

$$\begin{aligned} k0 &= C2 \bullet R2 \\ k1 &= C1 \bullet C2 \bullet C3 \bullet R2 \bullet R3 \\ k2 &= C2 \bullet C3 \bullet R2 + C1 \bullet C2 \bullet R2 + C1 \bullet C3 \bullet R3 + C2 \bullet C3 \bullet R3 \\ k3 &= C1 + C2 + C3 \end{aligned} \tag{1}$$

Then the transfer function of the loop filter is given by:

$$Z(s) = \frac{1 + s \bullet k0}{s \bullet \left[s^2 \bullet k1 + s \bullet k2 + k3 \right]} \tag{2}$$

This leads to the following closed-loop transfer function:

$$CL(s) = \frac{Kf \bullet Kvco \bullet N \bullet (1 + s \bullet k0)}{s^4 \bullet N \bullet k1 + s^3 \bullet k2 \bullet N + s^2 \bullet k3 \bullet N + s \bullet Kf \bullet Kvco \bullet k0 + Kf \bullet Kvco} \tag{3}$$

Second Order Approximation to Transient Response

To this point, no approximations have been made. In this section, CL(s) will be approximated by a second order expression, CL1(s), in order to derive results that give an intuitive feel of the transient response.

It is assumed that these higher order terms are small relative to the lower order terms. The Initial Value Theorem (4) suggests that the consequences of ignoring these terms are more on the initial characteristics, such as overshoot, and less on long time behavior, such as lock time.

$$\lim_{s \to \infty} s \bullet Y(s) = \lim_{t \to 0} y(t) \tag{4}$$

The simplified second order expression is:

$$CL1(s) = \frac{\left(\frac{Kf \bullet Kvco}{n \bullet k3} \right) \bullet \left(1 + s \bullet k0 \bullet N \right)}{s^2 + s \bullet \left(\frac{Kf \bullet Kvco \bullet k0}{k3 \bullet N} \right)} \tag{5}$$

Defining

$$wn = \sqrt{\frac{Kf \bullet Kvco}{N \bullet (C1 + C2 + C3)}} \tag{6}$$

$$z = \frac{R2 \bullet C2}{2} \bullet wn \tag{7}$$

It can be seen that the poles of this function are at:

$$-z \bullet wn \pm j \bullet wn \bullet \sqrt{1-z^2} \tag{8}$$

Now consider a PLL, which is initially locked at frequency ***f1***, and then the N counter is changed such to cause the PLL to switch to frequency ***f2***. It should be noted that the value for N that is used in all of these equations should be the value of N corresponding to ***f2***. This event is equivalent to changing the reference frequency from ***f1/N*** to ***f2/N***. The first term in the numerator of (5) shows the primary effects, and the second expression shows the secondary effects due to the zero. The zero in the transfer function has a lot of effect on the overshoot and the rise time, but has little effect on the lock time. Using inverse Laplace transforms it follows that the time frequency response is:

$$F(t) = f2 + (f1 - f2) \bullet e^{-z \bullet wn \bullet t} \bullet \left[\cos\left(wn\sqrt{1-z^2} \bullet t\right) + \frac{z - R2 \bullet C2 \bullet wn}{\sqrt{1-z^2}} \bullet \sin\left(wn\sqrt{1-z^2} \bullet t\right) \right] \tag{9}$$

Since the term in brackets has a maximum value of:

$$\frac{1 - 2 \bullet R2 \bullet C2 \bullet z \bullet wn + R2^2 \bullet C2^2 \bullet wn^2}{\sqrt{1-z^2}} \tag{10}$$

It follows that the lock time in seconds is given by:

$$Lock\,Time = \frac{-\ln\left(\frac{tol}{f2 - f1} \bullet \frac{\sqrt{1-z^2}}{1 - 2 \bullet R2 \bullet C2 \bullet z \bullet wn + R2^2 \bullet C2^2 \bullet wn^2} \right)}{z \bullet wn} \tag{11}$$

Many times, this is approximated by:

$$Lock\,Time = \frac{-\ln\left(\frac{tol}{f2 - f1} \bullet \sqrt{1-z^2} \right)}{z \bullet wn} \tag{12}$$

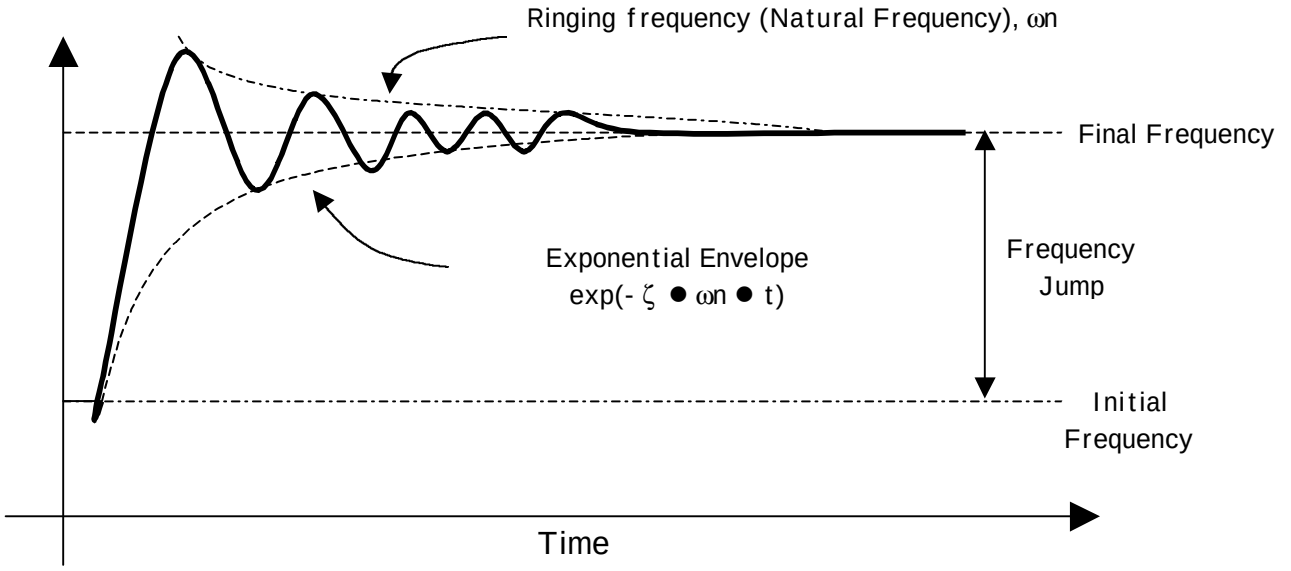


Figure 3 *Classical Model for the Transient Response of a PLL*

Figure 3 shows the classical second order model for the frequency response. For a second order filter, the following relationships exist for loop filters designed with National Semiconductor's AN-1001, National Semiconductor's online EasyPLL Program, or the equations presented in this book. These relationships are proven in the Appendix.

$$wc = 2 \bullet z \bullet wn$$
$$\sec f - \tan f = \frac{1}{4 \bullet z^2} \tag{13}$$

Phase Margin, ϕ	Damping Factor, ζ	Natural Frequency, ωn
30.00 degrees	0.6580	0.7599●ωc
35.00 degrees	0.6930	0.7215●ωc
36.87 degrees	0.7071	0.7071●ωc
40.00 degrees	0.7322	0.6829●ωc
45.00 degrees	0.7769	0.6436●ωc
50.00 degrees	0.8288	0.6033●ωc
55.00 degrees	0.8904	0.5615●ωc
60.00 degrees	0.9659	0.5177●ωc
61.93 degrees	1.0000	0.5000●ωc
65.00 degrees	1.0619	0.4709●ωc
70.00 degrees	1.1907	0.4199●ωc

Table 1 *Relationship Between Phase Margin, Damping Factor and Natural Frequency*

So by specifying a the loop bandwidth, ***wc***, and the phase margin, ***f***, the damping factor and natural frequency can be determined, and vise versa. Note here that ***wc*** is defined as the point where the magnitude of the open loop transfer function is equal to one.

$$\left\| \left. \frac{Kf \bullet Kvco \bullet Z(s)}{N \bullet s} \right|_{s = j \bullet wc} \right\| = 1 \tag{14}$$

Fourth Order Transient Analysis

This analysis considers all the poles and zeros of the transfer function, for a third order filter, and gives the most accurate results. It does require finding the roots of a fourth order polynomial. Although the formula is cumbersome, an explicit formula does exist for finding the roots. There also exists software, such as Mathcad, which is ideal for dealing with a problem such as this. In the case of a fourth order loop filter, this leads to a fifth order polynomial. Abel's Impossibility Theorem states that there can not exist a closed form solution for polynomials of fifth and higher order, so it is necessary to approximate this with a fourth order polynomial, or to find the roots numerically. The aim of this section is to derive an expression for the transient analysis that can be graphed and properties such as the lock time, rise time, overshoot, ringing, and damping factor can be seen from the graph. To start with, the transfer

function in (3) is multiplied by ***(f2-f1)/(Ns)***. However, since these formulas are really referring to the phase response, and it is the frequency response that is sought, the whole transfer function is also multiplied by ***s*** to perform differentiation (frequency is the derivative of phase). The resulting expression is rewritten in the following form:

$$\overline{F(s)} = s \bullet H(s) \bullet \frac{f2 - f1}{N \bullet s} = \frac{n1 \bullet (1 + s \bullet k0)}{s^4 + d3 \bullet s^3 + d2 \bullet s^2 + d1 \bullet s + d0} \tag{15}$$

where

$$n1 = \frac{Kf \bullet Kvco \bullet (f2 - f1)}{N \bullet C1 \bullet C2 \bullet C3 \bullet R2 \bullet R3} \tag{16}$$

$$d3 = \frac{k2}{k1} = \frac{C2 \bullet C3 \bullet R2 + C1 \bullet C2 \bullet R2 + C1 \bullet C3 \bullet R3 + C2 \bullet C3 \bullet R3}{R2 \bullet R3 \bullet C1 \bullet C2 \bullet C3} \tag{17}$$

$$d2 = \frac{k3}{k1} = \frac{C1 + C2 + C3}{R2 \bullet R3 \bullet C1 \bullet C2 \bullet C3} \tag{18}$$

$$d1 = \frac{Kf \bullet Kvco}{N \bullet C1 \bullet C3 \bullet R3} \tag{19}$$

$$d0 = \frac{Kf \bullet Kvco}{N \bullet R2 \bullet R3 \bullet C1 \bullet C2 \bullet C3} \tag{20}$$

Note that the roots of the denominator correspond to the poles of the transfer function. Since this is a fourth order polynomial, the roots of this function can be found analytically, although it is much easier to find them numerically. The transfer function can be rewritten as:

$$H(s) \bullet \frac{f2 - f1}{N \bullet s} = \sum_{i=0}^{3} A_i \bullet \left[\frac{1}{s \bullet (s - p_i)} + \frac{R2 \bullet C2}{s - p_i} \right] \tag{21}$$

$$A_i = n1 \bullet \prod_{k \neq i} \frac{1}{p_i - p_k} \tag{22}$$

Finally, this leads to the transient response. Note that some of the coefficients A_i will be complex; however, they will combine in such a way that the final solution is real. Now since the poles need to be calculated for this, it will be assumed that they all have negative real parts. If this is not the case, then the design is unstable. Using this assumption that the design is stable, the transient response can be simplified. Also, if the simulator does not do this, the solution can be expressed with all real variables by applying Euler's formula:

$$e^{a + j \bullet b} = e^a \bullet (\cos b + j \bullet \sin b) \tag{23}$$

Assuming a stable system, the transient response is:

$$F(t) = f2 + \sum_{i=0}^{3} A_i \bullet e^{p_i \bullet t} \bullet \left(\frac{1}{p_i} + R2 \bullet C2 \right) \tag{24}$$

Additional Comments Regarding the Lock Time Formula

Using the Exponential Envelope

Formula (24) provides a complete analysis for the transient response, including all of the ringing of the PLL. However, for the purposes of lock time determination, it is better to eliminate the ringing from the equation, and study only the exponential envelope. This makes the prediction of lock time more consistent. The exponential envelope is obtained by applying the triangle inequality to formula (24).

$$\textbf{Exponential Envelope} = f2 + \sum_{i=0}^{3} \left| A_i \bullet e^{p_i \bullet t} \bullet \left(\frac{1}{p_i} + R2 \bullet C2 \right) \right| \tag{25}$$

Cycle Slips

When an instantaneous phase error is presented to the phase detector, then cycle slipping can occur. When the N counter value changes, then the phase of the VCO signal divided by N will initially be incorrect in relation to the crystal reference signal divided by R. If the loop bandwidth is very small (around 1%) relative to the comparison frequency, then this phase error will accumulate faster than the PLL can correct for it and eventually cause the phase detector to put out a current correction of the wrong polarity. By dividing the comparison frequency by the instantaneous phase error presented to the phase detector, one can calculate how many cycles it would take the phase detector to cycle slip. If this time is less than about half the rise time of the PLL, then cycle slipping is likely to occur. An easier rule of thumb that is less accurate is that cycle slipping tends to occur when the loop bandwidth is less than 1% of the comparison frequency. Cycle slips are somewhat rare, but are most common fractional N PLLs, since they typically run at higher comparison frequencies.

Dependence of Lock Time on Loop Bandwidth

Although the filter design equations have not yet been presented, one fact will be borrowed from the design section in this book. Consider a two loop filters that are designed for the exact same parameters, except for the second loop filter is designed to have a loop bandwidth of K times the loop bandwidth of the first filter. In this case, all the resistor values in the second filter will be K times the resistor values in the first filter. Furthermore, the capacitors values in the second filter will be $1/K^2$ times the capacitor values of the first filter. If compares the values computed in formulas 15 through 21, one will find that if p which makes the denominator in equation (15) equal to zero for the first filter, then $K \bullet p$ will make the denominator in equation (15) equal to zero for the second filter. From formulas (16) and (22), one can see that the coefficients A_i are divided by a factor of K. Looking at formulas 24 or 25, the factors of K all cancel out, except in the exponent. This proves that the transient response for the second loop filter will be identical to that of the first, except for the time axis is scaled by a factor of $1/K$. The grand result of all this analysis is that it proves that the lock time is inversely proportional to the loop bandwidth, and that the overshoot (undershoot) will remain exactly the same.

Dependence of Lock Time on the Frequency Jump

The quantity $|f2 - f1|$ is the frequency jump. Now consider the same loop filter. For the first lock time measurement, the transient response is recorded. For the second lock time measurement, the final frequency, ***f2***, is kept constant, but the initial frequency, ***f1***, is changed such that the frequency jump is increased by a factor of ***K***., equation (24) and (25) will be the same for both cases, except for the fact that the coefficients for A_i in the second case will be multiplied by a factor of ***K***. This implies that the transient response will be the same for both cases, except for in the second case, the ringing is multiplied by a factor of ***K***. Note that although the lock time for the second case will be longer, it will be not be increased by a factor of ***K***, but rather something much less. What can be implied from this is that if the frequency jump and frequency tolerance are scaled by equal amounts, the lock time will be identical.

Rule of Thumb for Lock Time for an Optimized Filter

Although (24) is very complete, it is difficult to apply without the aid of computers. Simulations show optimal lock time occurs with a phase margin around 48 degrees. Recall that it was shown that lock time was inversely proportional to loop bandwidth, and that the lock time does not change if the frequency jump and frequency tolerance are scaled in equal amounts. Using the above rules and assuming 48 degrees of phase margin, a rule of thumb for lock time can be derived from simulated data.

$$LT \approx \frac{400}{Fc} \bullet \left(1 - \log_{10}(DF)\right)$$
$$DF = \frac{Frequency\,Tolerance}{Frequency\,Jump} \qquad (26)$$

LT is the lock time in microseconds, ***Fc*** is the loop bandwidth in KHz, and ***DF*** is the ratio as shown above.

Simulation Results

Figures 4 and 5 show a comparison between simulated results, based on this chapter, and actual measured data. There is very good agreement between these graphs. Note that the C2 capacitor in the loop filter was type CG0. When this was changed to a worse dielectric, the lock time increased from 489 μS to 578 μS. This example was also contrived so that the charge pump stayed away from the power supply rails, in order to eliminate the saturation effects of the charge pump. These are the effects that most often cause the measured result to differ from the theoretical result. The VCO capacitance was added to C3 for the purposes of the calculations.

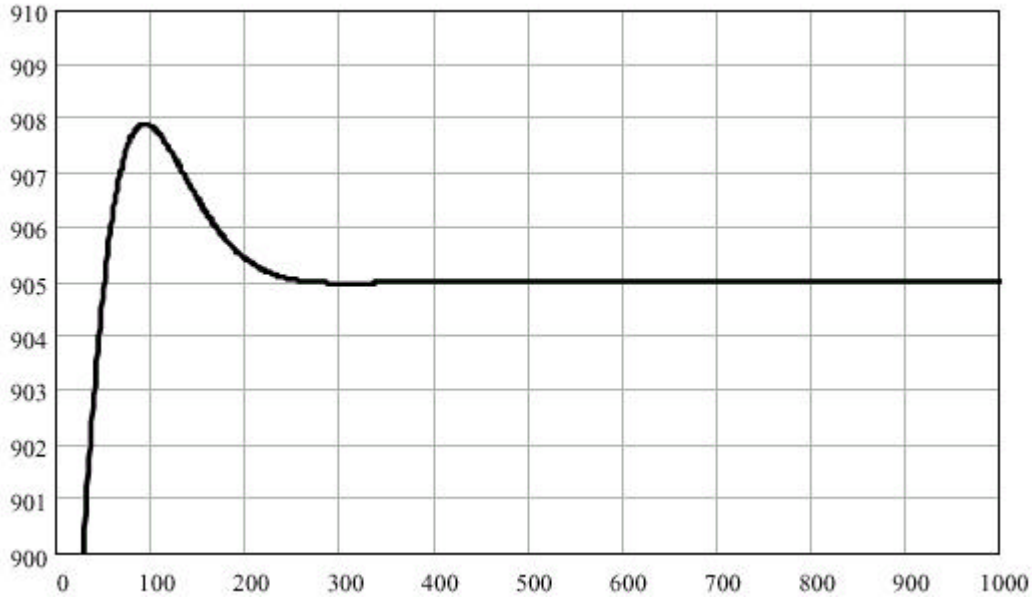


Figure 4a *Theoretical Peak Time of 94 mS to 907.9 MHz*

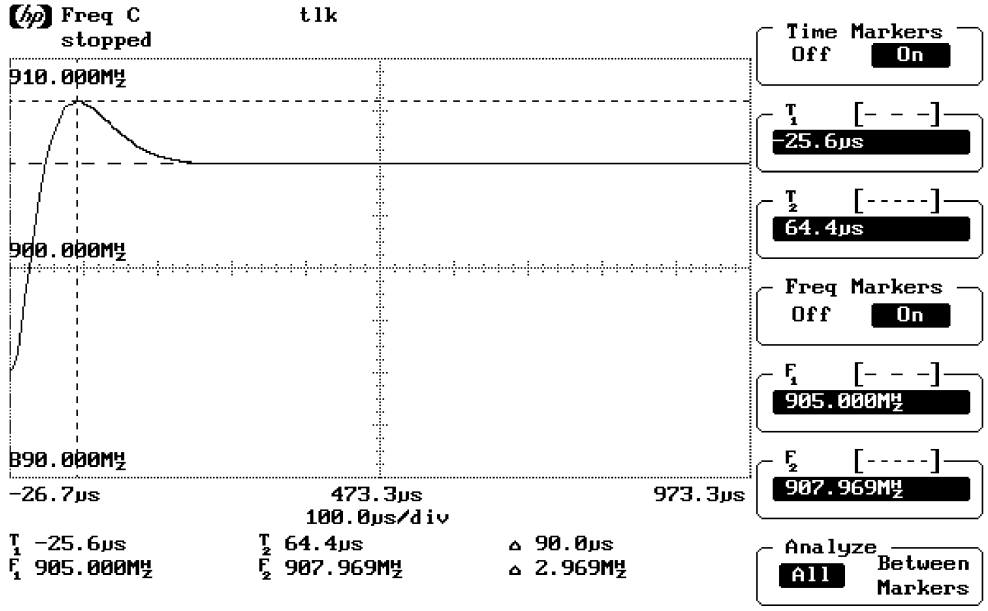


Figure 4b *Actual Peak Time of 90 uS to 908.0 MHz*

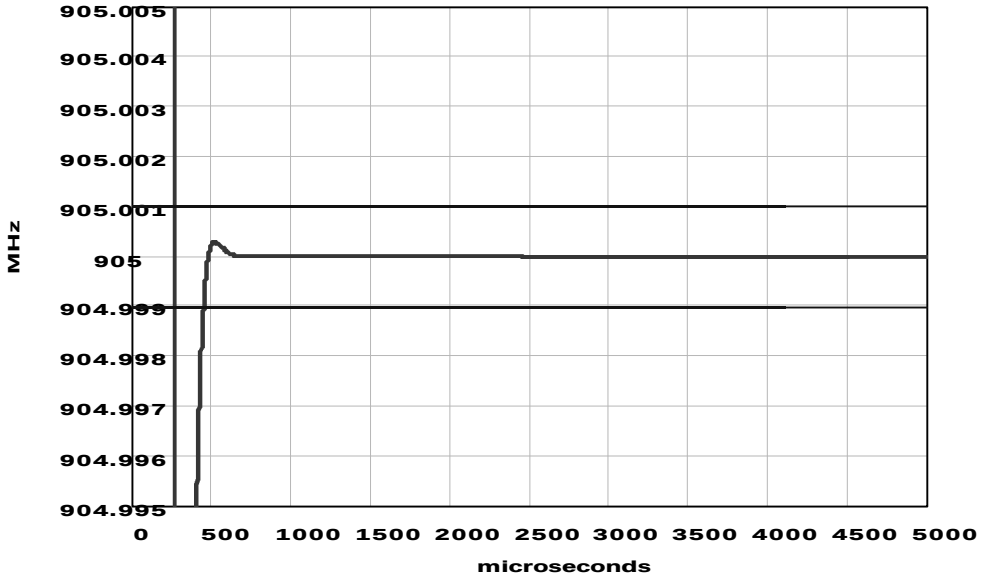


Figure 5a *Theoretical Lock Time to 1 KHz in 446 uS*

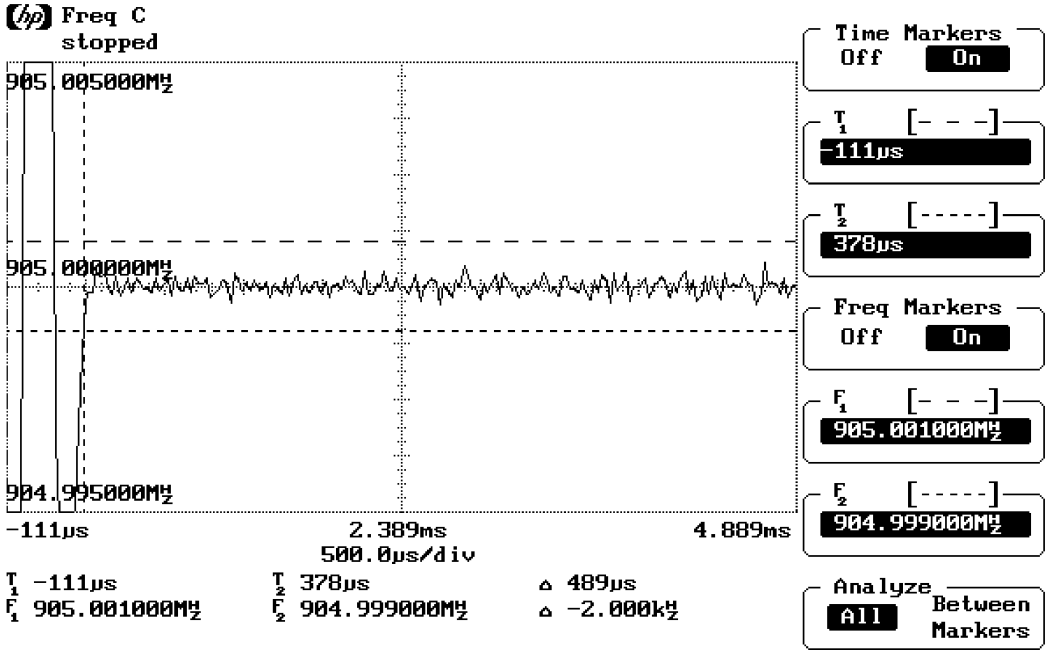


Figure 5b *Actual Lock time to 1 KHz of 489 uS*

Conclusion

This chapter has gone through a rigorous derivation of the equations involved in predicting lock time and the transient response of the PLL when the N divider is changed. A second order and a fourth order model were presented. For the fourth order model, discrepancies between theoretical lock times and measured lock times are on the order of 10 - 20 % or less. If theoretical lock times and measured lock times closely agree, then this indicates that this is the best the PLL can do. However, if there is a large discrepancy, then one or more of the factors below could be the cause.

VCO and Charge Pump Non-linearity

Perhaps the biggest real world effect that could throw off this analysis is the non-linear characteristics of the VCO and the charge pump. When switching from one frequency to another, there is typically overshoot in the order of one third of the frequency jump. This overshoot is dependent on the phase margin/damping factor. If the VCO overshoots too far past its intended range for usage, or if the tuning voltage ever gets too close (about 0.5 V) to the supply rails for the charge pump, the first lobe of the transient response gets longer and increases the lock time. The designer should be aware that if overshoot causes the frequency to go outside the tuning range of the VCO, the modeled prediction could lose accuracy. To deal with this, design for a higher phase margin in order to decrease the overshoot.

Not Accounting for the VCO Input Capacitance

The VCO input capacitance adds in parallel with the capacitor C3. If not accounted for, this could distort the results. This tends to decrease the loop bandwidth, and therefore increase the lock time.

Bad Capacitor Dielectrics

When larger capacitors, in the order of 1 nF or larger are used, cheaper capacitors, such as X7R can drastically increase lock times. By switching to higher quality capacitors, such as polypropylene, this can be fixed. If the actual lock time is substantially longer than the theoretical lock time, then replace the capacitors, especially capacitor C2, with ones of higher quality. For the example previously given, using a higher loss dielectric capacitor for component C2 increased the lock time from 489 μS to 578 μS.

Phase Detector Discrete Sampling Effects

The discrete sampling effects of the phase detector usually have little bearing on the lock time, provided that the comparison frequency is large (10 X) compared to the loop bandwidth. The fourth order model was compared to another model that did take into account these effects, and the difference in the lock time was very small. In an actual transient response for a PLL with a digital phase detector, there will be small jagged corrections corresponding to these corrections of the phase detector.

Other Comments

There are also charge pump mismatch, charge pump leakage, board parasitics, and component leakages that could cause additional errors. Although the equations for a fourth order loop filter were not presented here, the transient response can be derived in a very similar way that was used to derive the transient response for the third order loop filter.

Appendix

The Relationship Between Natural Frequency (wn), Damping Factor (z), Loop Bandwidth (wc) , and Phase Margin (f)

Note that since this is for a second order filter, C3 = R3 = 0. Recall from National Semiconductor's Application Note 1001, for a second order filter

$$T1 = \frac{\sec f - \tan f}{wc} \tag{27}$$

$$T2 = R2 \bullet C2 = \frac{1}{wc^2 \bullet T1} \tag{28}$$

Combining (5) , (6) , (27), and (28) in order to eliminate T1 and T2 yields the following:

$$\frac{wn}{z} = 2 \bullet wc \bullet (\sec f - \tan f) \tag{29}$$

Recall also from AN 1001

$$C2 = C1 \bullet \left(\frac{T2}{T1} - 1 \right) \tag{30}$$

This can be restated as follows,

$$C1 + C2 = \frac{T2}{T1} \bullet C1 \tag{31}$$

By AN 1001

$$C1 = \frac{T2}{T1} \bullet \frac{Kf \bullet Kvco}{N \bullet wc^2} \sqrt{\frac{1 + (wc \bullet T2)^2}{1 + (wc \bullet T1)^2}} \tag{32}$$

Substituting this expressing for C1 in the right hand side of (31), and equating this derived expression for C1+C2 obtained from equation (6) yields the following:

$$\frac{Kf \bullet Kvco}{N \bullet wc^2} \sqrt{\frac{1 + (wc \bullet T2)^2}{1 + (wc \bullet T1)^2}} = C1 + C2 = \frac{Kf \bullet Kvco}{N \bullet wn^2} \tag{33}$$

Using expressions (27) , (28) , and (29) in order to express T1 and T2 in terms of ζ, ωn, and ωp, yield the following equation:

$$\left(\frac{wc}{wn} \right)^4 = \frac{1 + \left(\frac{2 \bullet z \bullet wc}{wn} \right)^2}{1 + \left(\frac{wn}{2 \bullet z \bullet wc} \right)^2} \tag{34}$$

This equation can be simplified to an equation that is quadratic in wc^2 and can be solved using the quadratic formula for the following elegant relationship:

$$wc = 2 \bullet z \bullet wn \tag{35}$$

By substituting this into (29), the other relationship can be obtained

$$\sec f - \tan f = \frac{1}{4 \bullet z^2} \tag{36}$$

Note that no approximations were made for a second order filter. For a third order filter, these relationships are not exact, but serve as good approximations.

TRANSIENT ANALYSIS

$K\phi := 1 \cdot mA$ $Fcomp := 200kHz$ $Kvco := 18\frac{MHz}{volt}$

$C1 := 0.47nF$ $C2 := 10nF$ $C3 := 227pF$

$R2 := 8.2k\Omega$ $R3 := 27 \cdot k\Omega$

$f2 := 905MHz$ Final Frequency

$f1 := 895MHz$ Starting Frequency

$tol := 1000Hz$ Tolerance for Lock Time Measurments

Calculations

$R3 := \max\left(\begin{bmatrix} R3 \\ 1 \cdot \Omega \end{bmatrix}\right)$ $C3 := \max\left(\begin{bmatrix} C3 \\ 1 \cdot pF \end{bmatrix}\right)$ $N := \frac{f2}{Fcomp}$

$den2 := C1 + C2 + C3$

$den4 := R2 \cdot R3 \cdot C1 \cdot C2 \cdot C3$ $den3 := C2 \cdot C3 \cdot R2 + C1 \cdot C2 \cdot R2 + C1 \cdot C3 \cdot R3 + C2 \cdot C3 \cdot R3$

$den1 := \frac{K\phi \cdot Kvco \cdot C2 \cdot R2}{N}$ $num0 := \frac{K\phi \cdot Kvco \cdot (f2 - f1)}{N}$

$den0 := \frac{K\phi \cdot Kvco}{N}$ $num1 := num0 \cdot R2 \cdot C2$

$$v := \begin{bmatrix} \frac{den0}{den4} \cdot sec^4 \\ \frac{den1}{den4} \cdot sec^3 \\ \frac{den2}{den4} \cdot sec^2 \\ \frac{den3}{den4} \cdot sec \\ 1 \end{bmatrix} \qquad v = \begin{bmatrix} 1.684 \cdot 10^{19} \\ 1.384 \cdot 10^{15} \\ 4.529 \cdot 10^{10} \\ 5.136 \cdot 10^{5} \\ 1 \end{bmatrix}$$

These are the poles

$p := polyroots(v) \cdot sec^{-1}$

$$p = \begin{bmatrix} -4.115 \cdot 10^{5} \\ -5.835 \cdot 10^{4} \\ -2.189 \cdot 10^{4} - 1.49 \cdot 10^{4} i \\ -2.189 \cdot 10^{4} + 1.49 \cdot 10^{4} i \end{bmatrix} \cdot sec^{-1}$$

$$A_0 := \frac{\frac{num0}{den4}}{(p_0 - p_1)\cdot(p_0 - p_2)\cdot(p_0 - p_3)} \qquad A_0 = -3.137\cdot 10^{9}\ \text{sec}^{-2}$$

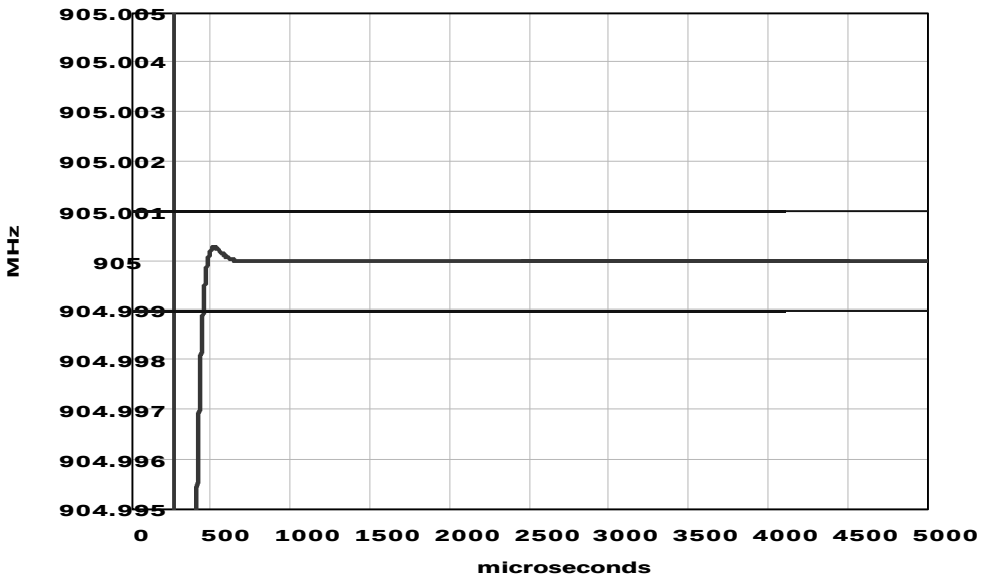
$$A_1 := \frac{\frac{num0}{den4}}{(p_1 - p_0)\cdot(p_1 - p_2)\cdot(p_1 - p_3)} \qquad A_1 = 3.074\cdot 10^{11}\ \text{sec}^{-2}$$

$$A_2 := \frac{\frac{num0}{den4}}{(p_2 - p_0)\cdot(p_2 - p_1)\cdot(p_2 - p_3)} \qquad A_2 = -1.524\cdot 10^{11} + 3.354\cdot 10^{11}\,i\ \text{sec}^{-2}$$

$$A_3 := \frac{\frac{num0}{den4}}{(p_3 - p_0)\cdot(p_3 - p_1)\cdot(p_3 - p_2)} \qquad A_3 = -1.524\cdot 10^{11} - 3.354\cdot 10^{11}\,i\ \text{sec}^{-2}$$

$k := 0 .. 5000$ $\qquad i := 0 .. 3$ $\qquad t_k := \frac{k}{1000000}\cdot\text{sec}$

$$F(t) := f2 + \sum_i A_i \cdot e^{p_i \cdot t_k}\left(\frac{1}{p_i} + R2\cdot C2\right)$$



$\text{LockTime} = 446\,\mu\text{sec}$ $\qquad \text{OverShoot} = 10\cdot\text{MHz}$

6. Discussions of the Phase/Frequency Detector for the Armchair Philosopher

Introduction

Perhaps the most difficult component to understand in the PLL system is the phase/frequency detector. It generates a signal that is proportional to the phase error. Since phase is the integral of frequency, it also gives some indication of the frequency error as well. In many older classical texts, devices such as mixers and XOR gates are mentioned as phase detectors. The mixer and XOR gate only worked within a limited range. This has caused a lot of confusion with the modern day phase frequency detector (PFD), which has no limitations on the operating range.

Looking carefully at Figure 1, it should be clear that the output is modeled as a phase and not a frequency. The VCO gain is divided by ***s***, which corresponds to integration. Recall this is done to convert the VCO frequency to a phase. If the frequency output is sought, then it is only necessary to multiply the transfer function by a factor of ***s***, which corresponds to differentiation. Now the phase-frequency detector not only causes the input phases to be equal, but also the input frequencies, since they are related.

Since phase is a little more abstract, many are interested in what the PFD does for two signals differing in frequency. This question is of particular interest in the construction of some lock detect circuits, where the average duty cycle of the phase detector is sought for a given frequency error. The reason that this chapter is directed towards the armchair philosopher is that thinking of the phase-locked loop in terms of frequencies is sufficient for most analysis, and many questions regarding phase tend to be very academic. This chapter investigates this question with an ideal phase/frequency detector with charge pump attached.

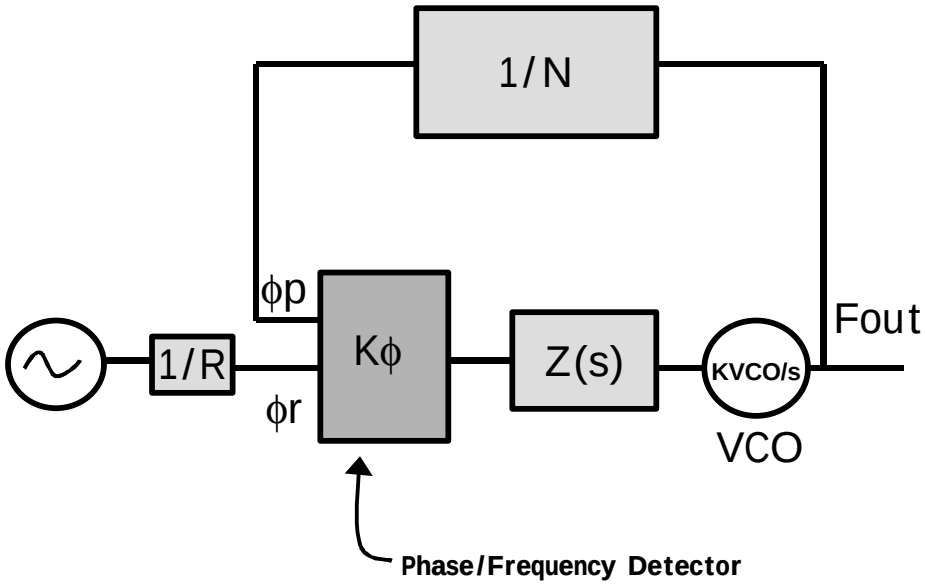


Figure 1 *The Basic PLL Structure Showing the Phase/Frequency Detector*

Analysis of the Phase/Frequency Detector

The output phase of the VCO is divided by N, before it gets to the Phase-Frequency Detector (PFD). Let ***fp*** represent the phase of this signal, and ***Fp*** represent the frequency of this signal. The output phase of the crystal reference is divided by R before it gets to the PFD. Let ***fr*** be the phase of this signal and Fr be the frequency of this signal. The PFD is only sensitive to the rising edges of ***fr*** and ***fp***. The PFD has the following three states:

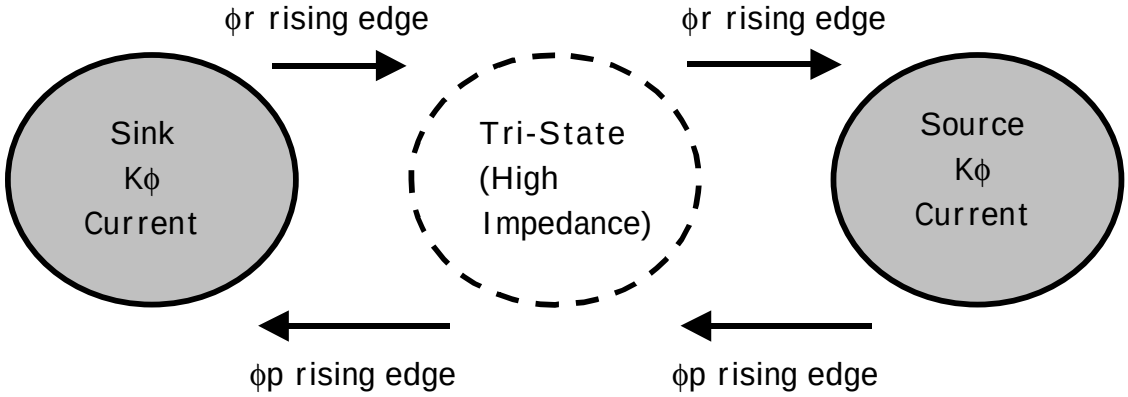


Figure 2 *States of the Phase Frequency Detector (PFD)*

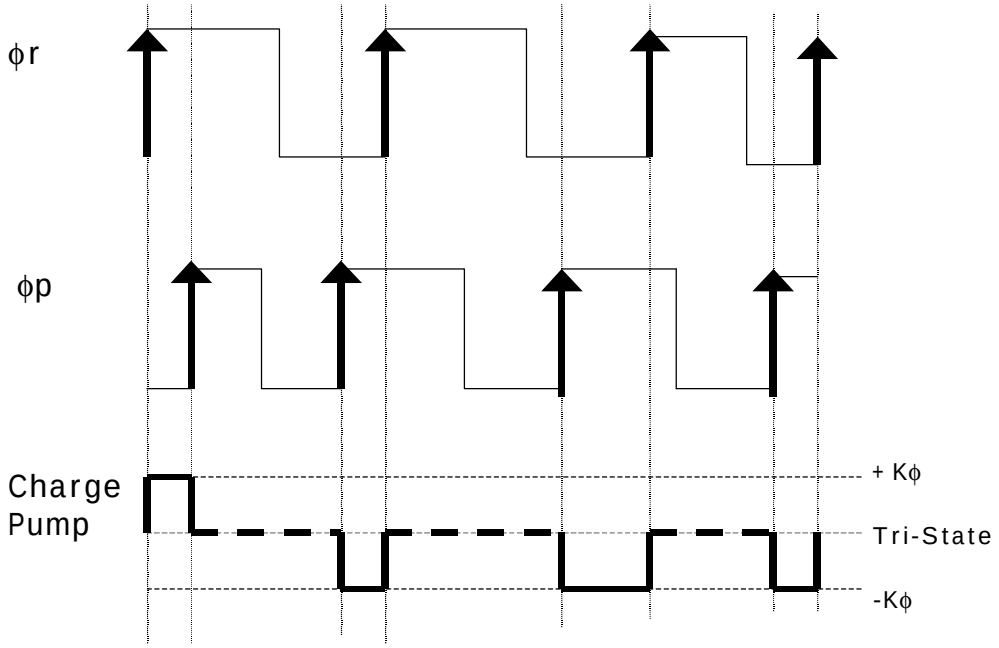


Figure 3 *Example of how the PFD works*

Analysis of the PFD for a Phase Error

Suppose that ***fp*** and ***fr*** are at the exact same frequency but off in phase such that the leading edge of ***fr*** is leading the leading edge of ***fp*** by a constant time period equal to ***t***. There are two cases that need to be covered.

t = 0: For this case, there is no phase error, and the signals are synchronized in frequency and phase, therefore there would theoretically be no output of the phase detector. In actuality, there would be some very small outputs from the phase detector due to dead zone elimination circuitry and gate delays of components. The charge pump output in this case is a series of positive and negative pulses, alternating in polarity.

t > 0: The charge pump will be on for a period of t for every reference period, $1/Fr$. Thus the average output of the charge pump would be:

$$t \bullet Fr \bullet Kf \tag{1}$$

But this delay period can be associated with a phase delay by multiplying by 2π. So it can be seen that the time averaged output of the PFD is proportional to the phase error. Note that for two signals of the same frequency, their phase difference can always be expressed as a number between 0 and 2π. Therefore, the difference, t, should always be less than $1/Fp$ in this case.

Phase Detector Gain

To calculate the phase detector gain note that it sources Kϕ current when the phase error is + 2π and sinks Kf current when the phase error is – 2π. Within this range, the curve is linear. This means that the proper phase detector gain is $Kf/2p$ (mA/rad). In design equations, the factor of 2π is often omitted because it is multiplied by another of 2π which is used to convert the VCO gain from MHz/volt to Mrad/volt.

Analysis of The PFD for Two signals Differing in Frequency and Phase

The phase detector has been analyzed for two signals differing in phase, but not for two signals differing in frequency. Although this analysis is sufficient for most situations, some may be interested in how the phase detector behaves for two signals differing in frequency. This is of particular interest in the construction of lock detect circuits. For the purposes of this analysis, the following terms will be defined:

Fr The frequency of the signal coming from the crystal reference and then divided by R
fp The phase of the fr signal at any given time
a The initial phase of the fr signal

Fp The frequency of the signal coming from the VCO and then divided by N
fp The phase of the fp signal at any given time
b The initial phase of the fr signal

t Elapsed time

Since frequency is the rate of change of the phase, it can be shown that:

$$fr = a + Fr \bullet t \tag{2}$$

$$fp = b + Fp \bullet t \tag{3}$$

Looking in this perspective, the phase difference is obvious, therefore the time-averaged output of the phase detector for any given time, t, would be:

$$Kf \bullet \left(a - b + (Fr - Fp) \bullet t\right) \tag{4}$$

Now the choice of t depends on whether or not $Fr>Fp$ or $Fr<Fp$. Without loss of generality, it will be assumed that $Fr>Fp$, if it is the other case, then a similar reasoning can be used. If one considers the average current output over P periods, this is shown below.

$$\begin{cases} \frac{Kf}{P} \bullet \left(a - b + (Fr - Fp) \bullet \frac{P}{Fr} \right) & Fr > Fp \\ \frac{Kf}{P} \bullet \left(a - b + (Fp - Fr) \bullet \frac{P}{Fp} \right) & Fr < Fp \end{cases} \tag{5}$$

Taking the limit as P approaches infinity gives the time-averaged output of the phase detector:

$$\begin{cases} Kf \bullet \left(1 - \frac{Fp}{Fr} \right) & Fr > Fp \\ Kf \bullet \left(1 - \frac{Fr}{Fp} \right) & Fr < Fp \end{cases} \tag{6}$$

When Fr is an integer multiple of Fp, these results in (6) have been verified by computer simulation. However, for smaller frequency errors, it has been verified that the charge pump output is a function of the ratio of Fr to Fp, and that this increases linearly with the frequency error for small frequency errors only. In a real situation, the PLL is tracking the phase error, which causes some of these simulations to be somewhat unrealistic. The equations above serve as a rough guess at the duty cycle of the phase detector for a given frequency error. In a closed loop system, the PLL is tracking the phase error, and this can cause these estimates to be a little different than theoretically predicted.

Other Information About the PFD

Continuous Time Approximation

The continuous time approximation approximates discrete current pulses from the phase detector as a continuous signal that has the same average value as the discrete pulses. This approximation becomes more rough as the comparison frequency approaches the loop bandwidth of the system. So, since the PLL charge pump puts out current pulses of magnitude Kf mA, the time averaged output of the charge pump would be $K\phi/2\pi$ mA/radian. Since the charge pump output $K\phi/2\pi$ multiplies the output of the VCO, $Kvco \bullet 2\pi$ in all of the equations involved in this chapter, the these factors of 2π cam be disregarded and pump output has been labeled as $K\phi$ and the VCO output can be labeled as Kvco. This approximation is used whenever transfer functions involving the phase detector gain are derived.

Discrete Sampling Effects on Loop Stability and Transient Response

The continuous time approximation holds when the loop bandwidth is small relative to the comparison frequency. If it is not, then theoretical predictions and actual results begin to differ and the PLL can even become unstable. Choosing the loop bandwidth to be $1/10^{th}$ of the comparison frequency is enough to keep one out of trouble, and when the loop bandwidth approaches around $1/3^{rd}$ the comparison frequency, simulation results show that this causes instability and the PLL to lose lock. In general, these effects should not be that much of a consideration.

Discrete Sampling Effects on Phase Noise

In terms of loop parameters and stability, these sampling effects are usually not that much of a concern, but they are very relevant in regards to phase noise. Recall that the phase detector/ charge pump tends to be the dominant noise source in the PLL and it is these discrete sampling effects that cause the PFD to be nosier at higher comparison frequencies. Since a PFD with a higher comparison frequency has more corrections, it also puts out more noise, and this noise is proportional to the number of corrections. It is for this reason that the PFD noise increases as ***10•log(Fcomp).***

Dead Zone Elimination Circuitry and Component Delays

The dead zone of the phase detector occurs around zero phase error. The problem that occurs here is that when the phase error is very small, the PFD is very non-responsive. There are also component delays. The dead zone elimination circuitry ensures that the phase detector always comes on for some amount of time to avoid operating in the dead zone.

Conclusion

This chapter has discussed the PFD (Phase Frequency Detector) and has given some characterization on how it performs for both frequency and phase errors. For the phase error, it can be seen that the output is proportional to the phase error. For frequency errors, it can be seen that there is some output that is positively correlated with the frequency error.

The PFD is named so because it can detect differences in both phase and frequency. It also bypasses many limitations that are part of using a mixer or XOR phase detector, such as pull-in range, hold-in range, and steady state phase error.

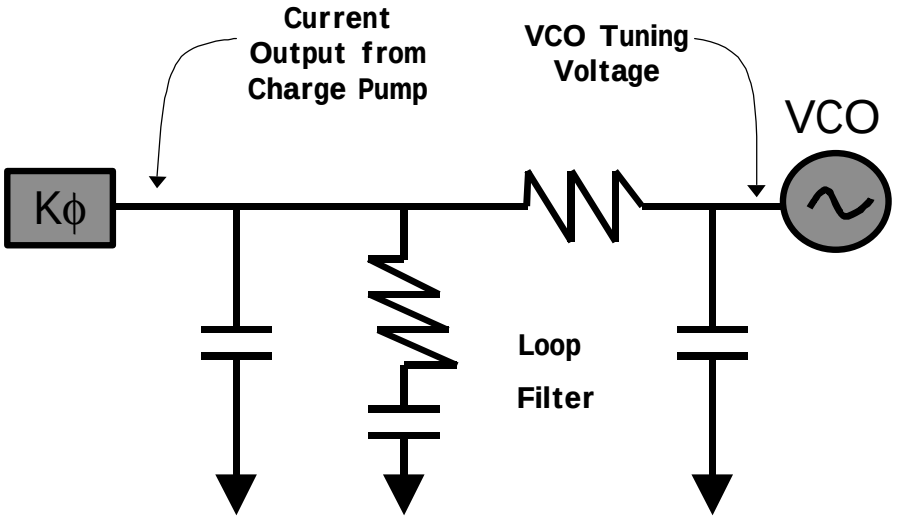
References

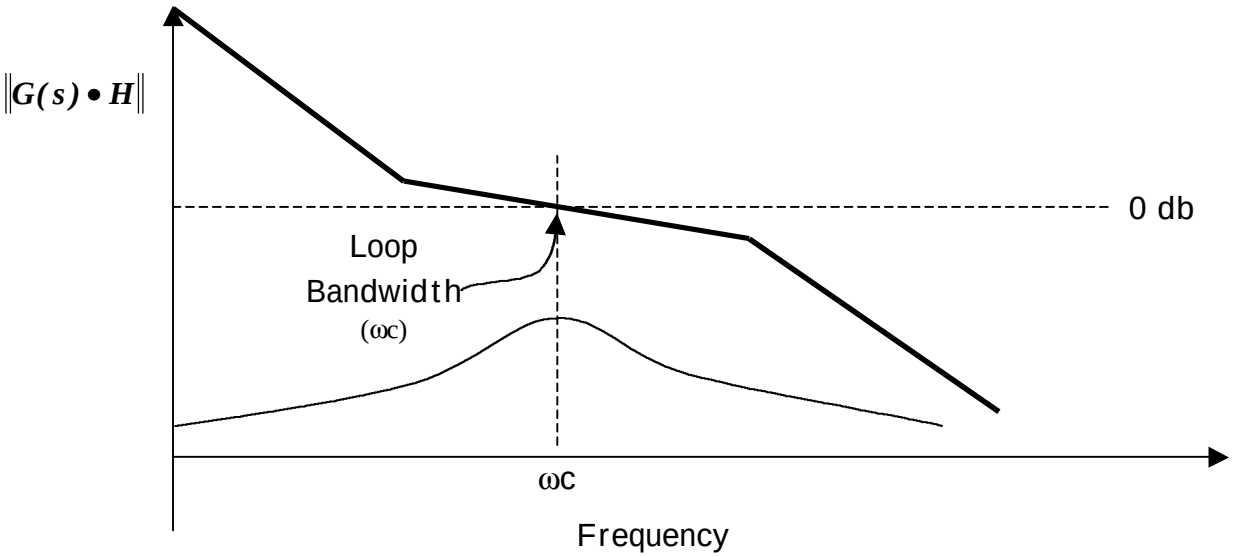
[1] Best, Roland E., *Phased Loop Theory, Design, Applications*, 3rd. ed, McGraw-Hill 1995

[3] Gardner, F.M. *Phased-Locked Loop Techniques*, 2nd ed., John Wiley & Sons, 1980

[4] Gardner, F.M., *Charge-Pump Phase-Lock Loops*, IEEE Trans. Commun. vol. COM-28, pp. 1849 – 1858, Nov 1980

PLL Design


Current
Output from
Charge Pump
VCO Tuning
Voltage
VCO
Kϕ
Loop
Filter


||G(s) • H||
0 db
Loop
Bandwidth
(ωc)
ωc
Frequency

7. Fundamentals of PLL Passive Loop Filter Design

Introduction

This chapter discusses the many technical issues that come with loop filter design. Loop filter design involves choosing the proper loop filter topology, loop filter order, phase margin, loop bandwidth, and pole ratios. Once these are chosen, the poles and zero of the filter can be determined. From these, the loop filter components can then be calculated. This chapter discusses the fundamental principles that are necessary for an understanding of loop filter design.

Determining the Loop Filter Topology and Order

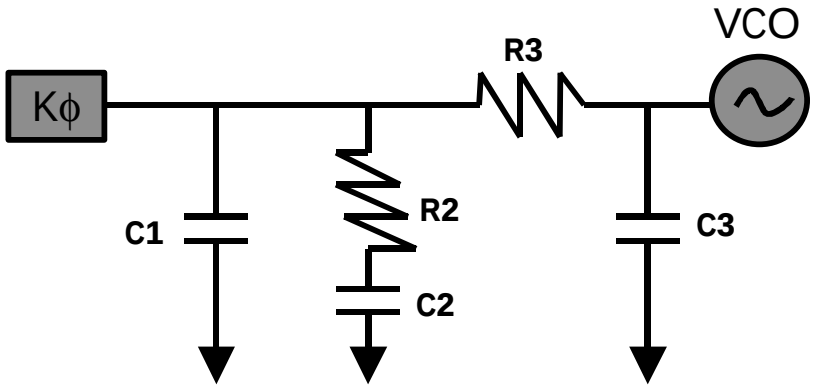


Figure 1 *A Third Order Passive Loop Filter*

A third order passive loop filter is show above. Passive loop filters are usually recommended above active loop filters, because adding active devices adds phase noise, complexity, and cost. However, there are cases where an active filter is necessary. The most common case arises when the maximum PLL charge pump voltage is lower than the VCO tuning voltage requirements. If higher tuning voltages are supplied to a VCO, then either the tuning range can be expanded or the phase noise reduced.

In terms of filter order, the most basic is the second order filter. Additional RC low pass filtering stages can be added to reduce the reference spurs. The impact of adding these additional stages is discussed in other chapters. In Figure 1, R3 and C3 form an additional low pass filtering stage.

Choosing the Phase Margin, Loop Bandwidth, and Pole Ratios

The phase margin (f) relates to the stability of a system. This parameter is typically chosen between 40 and 55 degrees. Simulations show that a phase margin of about 48 degrees yields the optimal lock time. Higher phase margins may decrease peaking response of the loop filter at the expense of degrading the lock time. For minimum RMS phase error designs, 50 degrees is a good starting point for phase margin.

The loop bandwidth (wc) is the most critical parameter of the loop filter. Choosing the loop bandwidth too small will yield a design with improved reference spurs and RMS phase error, but all at the expense of increased lock time. Choosing the loop bandwidth too wide will result in improved lock time at the expense of increased reference spurs and RMS phase error. The suggested method of choosing the loop bandwidth is to choose it so that it is sufficient to

meet the lock time requirement with sufficient margin. In cases where there is no lock time requirement, then it makes sense to choose the loop bandwidth at the frequency where the PLL noise equals the VCO noise for an optimal RMS phase error design. For a minimum reference spur design, the narrower the loop bandwidth, the lower the spurs. However, at some point the loop filter component values will be come unrealistically large.

The pole ratios (***T31***, ***T41***, ..) have less impact on the design than the loop bandwidth, but still are important. They tell the ratio of each pole, relative to the pole T1, for instance:

T1 = ***T11•T1*** *(Note T11 is trivial and always equal to 1)*
T3 = ***T31•T1***
T4 = ***T41•T1***

It will be shown in a later chapter that choosing all pole ratios to be one is theoretically the lowest reference spur solution. However, choosing them smaller can make sense when the capacitor in the loop filter next to the VCO is not at least three times the VCO input capacitance (typically 10 – 100 pF). The impact of the pole ratios on the reference spurs is explained in depth in another chapter.

The Loop Filter Impedance and Open Loop Gain

The loop filter impedance is defined as the output voltage at the VCO divided by current injected at the PLL charge pump. The expression for the loop filter impedance and the corresponding poles and zeros are shown below for various filter orders.

$$Z(s)=\frac{1+s\bullet T2}{Ctot\bullet s\bullet(1+s\bullet T1)\bullet(1+s\bullet T3)\bullet(1+s\bullet T4)} \tag{1}$$

Parameter	Second Order Filter	Third Order Filter	Fourth Order Filter
T1	$\frac{R2\bullet C2\bullet C1}{Ctot}$	$\frac{R2\bullet C2\bullet C1}{Ctot}$*	$\frac{R2\bullet C2\bullet C1}{Ctot}$*
T2	R2•C2	R2•C2	R2•C2
T3	0	R3•C3*	R3•C3*
T4	0	0	R4•C4*
Ctot	C1 + C2	C1 + C2 + C3	C1 + C2 + C3 + C4

* *This indicates this formula is approximate, not exact*

Table 1 *Impedance Parameters for Various Filter Orders*

Once the impedance (***Z(s)***), charge pump gain (***Kf***), and VCO Gain (***Kvco***) are known, then the open loop gain (***G(s)***)is given below:

$$G(s)=\frac{Kf\bullet Kvco}{s}\bullet Z(s) \tag{2}$$

Determining the Time Constants

This method of determining the poles and zeros is taken from reference [1]. The phase margin is specified as 180 degrees plus the phase of the forward loop gain, where the forward loop gain is specified as the open loop gain divided by the N divider value. Therefore it is true that:

$$f=180+\arctan(wc\bullet T2)-\arctan(wc\bullet T1)-\arctan(wc\bullet T1\bullet T31)-\arctan(wc\bullet T1\bullet T41) \tag{3}$$

Since f and the pole ratios are known, then this can be simplified to an expression involving ***T1*** and ***T2***. A second expression involving ***T1*** and ***T2*** can be found by setting the derivative of the phase margin equal to zero at the frequency equal to the loop bandwidth. This maximizes the phase margin at this frequency. Simulations show that satisfying this condition minimizes the lock time of the PLL for second order filter.

$$\left.\frac{df}{dw}\right|_{w=wc} = 0 = \frac{wc \bullet T2}{1+wc^2 \bullet T2^2} - \frac{wc \bullet T1}{1+wc^2 \bullet T1^2} - \frac{wc \bullet T1 \bullet T31}{1+wc^2 \bullet T1^2 \bullet T31^2} - \frac{wc \bullet T1 \bullet T41}{1+wc^2 \bullet T1^2 \bullet T41^2} \quad (4)$$

Equations (3) and (4) present a system of two equations with two unknowns (***T1*** and ***T2***). The solution to these equations is presented in chapters to come. This system can always be solved numerically and in the case of a second order filter (***T3*** = ***T4*** = ***0***), an elegant closed form solution exists.

Although simulations show that maximizing the phase margin at the loop bandwidth provides optimal lock times for second order filters, it turns out that this constraint is not the one which yields optimal lock times for higher order filters. However, this constraint does serve as a good approximation for third and higher order loop filters.

Calculating the Components from the Time Constants

Calculating the Total Loop Filter Capacitance

This is the step that is expanded in much greater detail in other chapters. However, one common concept that arises, regardless of the filter order, is the total capacitance. This is just the sum of all the capacitance values in the loop filter. If one considers a delta current spike, then it should be intuitive that in the long term, the voltages across all the capacitors should be the same and that its voltage would be the same as if all four capacitors values were added together. The final value theorem says this result can be found by taking the limit of ***s•Z(s)*** as ***s*** approaches zero. This result is ***Ctot***, the total loop filter capacitance.

Ctot can be found by setting the forward loop gain (***G(s)*** divided by N) equal to one at the loop bandwidth.

$$Ctot = \frac{Kf \bullet Kvco}{N \bullet wc^2} \bullet \sqrt{\frac{\left(1+wc^2 \bullet T2^2\right)}{\left(1+wc^2 \bullet T1^2\right) \bullet \left(1+wc^2 \bullet T3^2\right) \bullet \left(1+wc^2 \bullet T4^2\right)}}$$

Concerns with the VCO Input Capacitance

The VCO will have an input capacitance, typically on the order of 10 – 100 pF, which will add to the capacitances of the loop filter. This often becomes an issue with third and higher order loop filter designs, because the capacitor shunt with the VCO should be at least three times the VCO input capacitance to keep it from distorting the performance of the loop filter. In order to maximize this capacitance, design for the highest charge pump setting.

Concerns with Resistor Thermal Noise

The resistors in the loop filter, particularly the ones in the low pass RC filters (R3, R4, ..) generate thermal noise, which can increase the phase noise at and outside of the loop bandwidth. This starts to become a factor when these resistances are bigger than about 10 KΩ, although this is design specific. Designing for a higher charge pump current minimizes the loop filter resistors and thermal noise.

Conclusion

The equations to explicitly solve for the component values are presented in upcoming chapters, but they are all derived from these fundamental concepts and formulas presented in this chapter. The second order filter is a special case where ***T3*** = ***T4*** = ***0***. The third order filter is a special case where ***T3>0*** and ***T4 = 0***. These formulas could be easily generalized for filters of higher than fourth order, but this is more of an academic exercise than something of practical value. Note that some textbooks show a similar filter topology as presented in this chapter, except that ***C1 = 0***. Although this is a stable loop filter design, this topology is not recommended, because the reference spur attenuation is not as good.

References

[1] Keese, William O. *An Analysis and Performance Evaluation of a Passive Filter Design Technique for Charge Pump Phased Locked Loops* Application Note 1001. National Semiconductor

8. Equations for a Passive Second Order Loop Filter

Introduction

The second order loop filter is the least complex loop filter and allows one to explicitly solve for the component values in closed form. The second order filter has the smallest resistor thermal noise and largest capacitor next to the VCO to minimize the impact of VCO input capacitance. This filter also has maximum resistance to variations in VCO gain and charge pump gain. In cases where the first spur to be filtered is less than 10 times the loop bandwidth frequency, filter orders higher than third order do not provide much real improvement in spur levels. For the second order filter ***T3 = T4 = T31 = T41 = 0***.

Loop Filter Impedance, Pole, and Zero

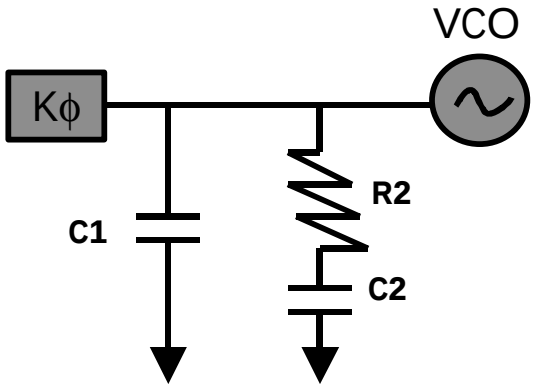


Figure 1 *A Second Order Passive Loop Filter*

The impedance of a second order loop filter is given below:

$$Z(s) = \frac{1 + s \bullet C2 \bullet R2}{s \bullet (C1 + C2) \bullet \left(1 + s \bullet \frac{C1 \bullet C2 \bullet R2}{C1 + C2}\right)} = \frac{1 + s \bullet T2}{s \bullet Ctot \bullet (1 + s \bullet T1)} \tag{1}$$

From the above equation, it should be clear:

$$\begin{aligned} T2 &= R2 \bullet C2 \\ T1 &= \frac{R2 \bullet C2 \bullet C1}{Ctot} \\ Ctot &= C1 + C2 \end{aligned} \tag{2}$$

From chapter 7, a system of two equations and two unknowns can be established by calculating the phase margin and also setting the derivative of the phase margin equal to zero at the loop bandwidth.

$$f = 180 + \arctan(wc \bullet T2) - \arctan(wc \bullet T1) \tag{3}$$

$$\left.\frac{df}{dw}\right|_{w=wc} = 0 = \frac{wc \bullet T2}{1+wc^2 \bullet T2^2} - \frac{wc \bullet T1}{1+wc^2 \bullet T1^2} \tag{4}$$

Equation (4) can be solved and has the solution:

$$wc \bullet T2 = \frac{1}{wc \bullet T1} \tag{5}$$

Substituting (6) into (4), taking the tangent of both sides, and solving yields:

$$T1 = \frac{sec(f) - tan(f)}{wc} \tag{6}$$

The time constant T2 can now be easily found using equation (5). The total loop filter capacitance, ***Ctot***, can be found by using the method presented in chapter 7, and C1 can be calculated.

$$Ctot = \frac{C1 \bullet T2}{T1} = \frac{Kf \bullet Kvco}{N \bullet wc^2} \bullet \sqrt{\frac{\left(1+wc^2 \bullet T2^2\right)}{\left(1+wc^2 \bullet T1^2\right)}}$$

Once the total capacitance is known, the components can be easily found:

$$\Rightarrow C1 = Ctot \bullet \frac{T1}{T2}$$
$$\Rightarrow C2 = Ctot - C1$$
$$\Rightarrow R2 = \frac{T2}{C2}$$

Conclusion

The formulas for the second order passive loop filter have been presented in this chapter. These formulas are just a special case of the formulas presented in a previous chapter. The second order filter has an elegant solution for the component values, but higher order filters may have lower reference spurs. A particular topology of loop filter was assumed in this chapter. There is actually another topology for the second order filter that is sometimes used in active filters. For different topologies, the component values may change, but the formulas for the time constants remain the same.

References

[1] Keese, William O. *An Analysis and Performance Evaluation of a Passive Filter Design Technique for Charge Pump Phased Locked Loops*

A SECOND ORDER LOOP FILTER DESIGN

USER NEEDS TO ENTER THESE

$\phi := 50\,deg$ Phase margin

$Fc := 10\,kHz$ Loop Bandwidth

$Fcomp := 200\,kHz$ Comparison Frequency

$Kvco := 20\frac{MHz}{volt}$ VCO Gain

$K\phi := 5\cdot mA$ Phase Detector Gain

$Fout := 2450\,MHz$ RF output frequency.

BASIC CALCULATIONS

$$N := \frac{Fout}{Fcomp} \qquad \omega c := 2\cdot\pi\cdot Fc$$

CALCLUATE POLE AND ZERO

$$T1 := \frac{\left(\frac{1}{\cos(\phi)}\right) - \tan(\phi)}{\omega c} \qquad T2 := \frac{1}{\omega c^2\cdot T1}$$

$T1 = 5.798\cdot 10^{-6}\,sec$ $T2 = 4.378\cdot 10^{-5}\,sec$

CALCULATE COMPONENTS FROM POLES AND ZERO

$$Ctot := \frac{K\phi\cdot Kvco}{\omega c^2\cdot N}\cdot\left[\frac{1+\omega c^2\cdot T2^2}{(1+\omega c^2\cdot T1^2)}\right]^{\frac{1}{2}} \qquad Ctot = 5.681\,nF$$

$C1 := \frac{T1}{T2}\cdot Ctot$ $C1 = 0.753\,nF$

$C2 := Ctot - C1$ $C2 = 4.929\,nF$

$R2 := \frac{T2}{C2}$ $R2 = 8.879\,k\Omega$

LOOP FILTER ANALYSIS

CALCULATE TRUE POLES AND ZERO

$T2 := R2 \cdot C2$ $\qquad$ $T1 := \frac{R2 \cdot C2 \cdot C1}{C1 + C2}$

Time Constant	Filter Pole	Filter Zero
$T1 = 5.796 \times 10^{-6}\ sec$	$\frac{1}{T1} = 172.62\ kHz$	n/a
$T2 = 4.378 \times 10^{-5}\ sec$	n/a	$\frac{1}{T2} = 22.86\ kHz$

DEFINE LOOP PARAMETERS

$Z(\omega) := \frac{1 + T2 \cdot i \cdot \omega}{i \cdot \omega \cdot (C1 + C2) \cdot (1 + i \cdot \omega \cdot T1)}$ Loop Filter Impedance

$G(\omega) := \frac{K\phi \cdot Kvco \cdot Z(\omega)}{i \cdot \omega}$ Forward Loop Gain

LOOP BANDWIDTH AND PHASE MARGIN

$\omega := 1.0kHz$

$\omega c := root(|G(\omega)| - N, \omega)$ $\quad \frac{\omega c}{2 \cdot \pi} = 10\ kHz$ Loop Bandwidth

$\omega := \omega c$

$arg(G(\omega c)) \cdot \frac{180}{\pi} + 180 = 50$ Phase Margin

9. Equations for a Passive Third Order Loop Filter

Introduction

In cases where the spur to be filtered is more than ten times the loop bandwidth, a third order filter can provide some benefit. Unlike the second order loop filter, there is no closed form solution for the exact component values. Designing the loop filter involves solving for the time constants, and then determining the loop filter components from the time constants. The time constants can be calculated either by introducing approximations and writing down a closed form approximate solution, or using numerical methods to solve more precisely for the time constants. Once the time constants are found, the component values can also be calculated approximately by introducing approximations, or exactly using numerical methods.

The method of introducing approximations to solve for the time constants and components will be referred to the standard method, and the method of using numerical methods to solve exactly (at least within very fine tolerances) will be referred to as the exact method.

Note that in addition to specifying the loop bandwidth, ***wc***, and phase margin, ***f***, the user also has to specify the pole ratio, ***T31***. This parameter can range from zero to one. A good starting value for this parameter is 0.8.

Calculating the Loop Filter Impedance and Time Constants

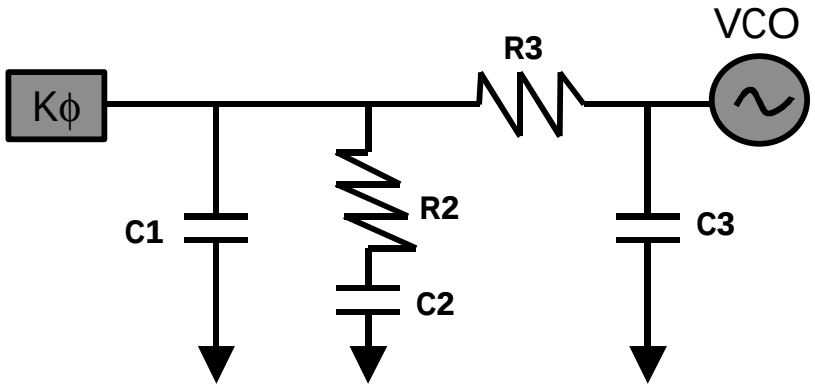


Figure 1 *Third Order Passive Loop Filter*

For the loop filter shown in Figure 1, the impedance is given below:

$$Z(s) = \frac{1 + s \bullet T2}{s \bullet Ctot \bullet (1 + s \bullet T1) \bullet (1 + s \bullet T3)} = \tag{1}$$

$$\frac{1 + s \bullet C2 \bullet R2}{s \bullet (s^2 \bullet C1 \bullet C2 \bullet C3 \bullet R2 \bullet R3 + s \bullet [C2 \bullet R2 \bullet (C1 + C3) + C3 \bullet R3 \bullet (C1 + C2)] + Ctot}$$

The following parameters are exact:

$$\begin{aligned} T2 &= R2 \bullet C2 \\ Ctot &= C1 + C2 + C3 \end{aligned} \tag{2}$$

The time constants can be calculated exactly by setting up a system of two equations and two unknowns, or by introducing the following approximations:

$$T1 = \frac{R2 \bullet C2 \bullet C1}{Ctot}$$
$$T3 = R3 \bullet C3 \tag{3}$$

These approximations hold provided:

$$\frac{C1}{C3} >> 1 - \frac{T3}{T2} \tag{4}$$

It will be shown in later chapters that ***T1*** + ***T3*** < ***T2*** is required for stability, so the approximations for the time constants should be realistic provided ***C3*** < ***C1/5***.

Standard Loop Filter Calculation

Calculation of Time Constants

Although the standard method of time constant calculation requires more work to derive the formulas, these formulas are easier to apply once they are derived. Since the standard method introduces approximations to solve for the time constants, the phase margin will not be exactly maximized at the loop bandwidth, but it should be pretty close.

By setting the derivative of the phase margin equal to zero, the following relationship is obtained:

$$\left.\frac{df}{dw}\right|_{w=wc} = 0 = \frac{wc \bullet T2}{1 + wc^2 \bullet T2^2} - \frac{wc \bullet T1}{1 + wc^2 \bullet T1^2} - \frac{wc \bullet T1 \bullet T31}{1 + wc^2 \bullet T1^2 \bullet T31^2} \tag{5}$$

By dividing through by ***wc***, finding a common denominator, and applying the assumption, ***T2*** >> ***T1*** + ***T3***, the following approximate relationship for ***T2*** can be found.

$$T2 \approx \frac{1}{wc^2 \bullet (T1 + T3)} \tag{6}$$

The phase margin is given by:

$$f = \tan^{-1}(wc \bullet T2) - \tan^{-1}(wc \bullet T1) - \tan^{-1}(wc \bullet T3) \tag{7}$$

From here, three trigonometric identities are needed:

$$\begin{aligned} \tan(p + x) &= \tan(x) \\ \tan(x) &\approx x \quad (\text{if } x \text{ is small}) \\ \tan^{-1}(x) &\approx x \quad (\text{if } x \text{ is small}) \end{aligned} \tag{8}$$

By substituting (6) into (7), applying the tan function to both sides, and applying the three above identities (assuming ***wc•T1*** and ***wc•T3*** to be small) yields the following simplification:

$$T1 + T3 \approx \frac{\sec(f) - \tan(f)}{wc} \tag{9}$$

The two poles in the loop filter can therefore be found as follows:

$$T1 \approx \frac{\sec(f) - \tan(f)}{wc \bullet (1 + T31)}$$
$$T3 = T1 \bullet T31 \tag{10}$$

Solution of Component Values from Time Constants

The choice of ***C3*** is somewhat arbitrary, but should be no larger than ***C1/5*** in order to justify the approximations for the time constants ***T1*** and ***T3***. Because the VCO input capacitance (10 – 100 pF) adds in parallel to ***C3*** and ***R3*** causes thermal noise outside the loop bandwidth, it is desirable to choose ***C3*** as large as possible without violating any constraints. For the equations below, ***C1*** was chosen to be equal to ***C1/5***. In cases where ***C3*** is much larger than the VCO input capacitance, and ***R3*** is small, then it makes sense to choose ***C3*** smaller than ***C1/5*** to better justify the loop filter approximations made. In an analogous way as done in the second order filter, the components can be calculated

$$
\begin{aligned}
Ctot &= \frac{Kf \bullet Kvco}{wc^2 \bullet N} \bullet \sqrt{\frac{1+wc^2 \bullet T2^2}{\left(1+wc^2 \bullet T1^2\right)\bullet\left(1+wc^2 \bullet T3^2\right)}} \\
C1 &= \frac{T1}{T2} \bullet Ctot \\
C3 &= \frac{C1}{5} \\
C2 &= Ctot - C1 - C3 \\
R2 &= \frac{T2}{C2} \\
R3 &= \frac{T3}{C3}
\end{aligned}
\tag{11}
$$

Exact Method of Loop Filter Calculation

To calculate the loop filter components without approximations, ***T1*** and ***T3*** now correspond to the true poles of the filter, as was not the case before. It is also possible to use the method in the previous section to solve approximately for the time constants, and then the method in this section to solve for the loop filter components and relaxes the restriction that ***C3>C1/5***.

True Loop Filter Impedance

The true impedance of the filter is given by:

$$
Z(s) = \frac{1+s \bullet T2}{s \bullet (1+s \bullet T1) \bullet (1+s \bullet T3)} \bullet \frac{1}{Ctot} \tag{12}
$$

And the time constants are determined by:

$$
\begin{aligned}
T2 &= \quad 2 \bullet C2 \\
T1 + \quad 3 &= \frac{C2 \bullet C3 \bullet \quad 2 + C1 \bullet C2 \bullet \quad 2 + C1 \bullet C3 \bullet \quad 3 + C2 \bullet C3 \bullet \quad 3}{C1 + C2 + \quad 3} \\
\frac{T1 \bullet T3}{2} &= \frac{C1 \bullet C3 \bullet \quad 3}{C1 + C2 + \quad 3}
\end{aligned}
\tag{13}
$$

Exact Method for Solving for the Time Constants T1 and T2
Choosing the loop bandwidth to maximize the phase margin yields

$$\frac{wc \bullet T2}{1+(wc \bullet T2)^2} = \frac{wc \bullet T1}{1+(wc \bullet T1)^2} + \frac{wcT1 \bullet T31}{1+(wc \bullet T1 \bullet T31)^2} = f(wc \bullet T2) \tag{14}$$

$$wc \bullet T2 = \frac{1 \pm \sqrt{1-4 \bullet f(wc \bullet T1)^2}}{2 \bullet f(wc \bullet T1)} = g(wc \bullet T1) \tag{15}$$

In (15) it has been found by trial and error that the positive root usually makes the math work out in the end. However, it may be possible that using the negative root could yield better results in some cases.

Using (15) and (7) to eliminate ***wc•T2*** yields:

$$f = p + \tan^{-1}(g(x)) - \tan^{-1}(x) - \tan^{-1}(x \bullet T31) \tag{16}$$

Since x is the only unknown, this equation can be solved numerically for ***x*** and then ***T1*** can be found via the equation:

$$T1 = \frac{x}{wc} \tag{17}$$

Once ***T1*** is known, ***T2*** can be found by

$$T2 = \frac{g(wc \bullet T1)}{wc} \tag{18}$$

Calculation of Component Values from Time Constants Using the Exact Method
Now, by definition, the gain of the open loop transfer function is equal to one at the loop bandwidth. Therefore ...

$$C1+C2+C3 = Ctot = \frac{Kf \bullet Kvco}{wc^2 \bullet N} \bullet \sqrt{\frac{1+(wc \bullet T2)^2}{(1+(wc \bullet T1)^2) \bullet (1+(wc \bullet T3)^2)}} \tag{19}$$

Defining a system of four equations and four unknowns
This leads to a system of four equations and four unknowns:

Constants

$$\begin{aligned} k1 &= Ctot \\ k2 &= (T1+T3) \bullet k1 \\ k3 &= \frac{T1 \bullet T3 \bullet k1}{T2} \\ k4 &= \frac{C3}{C1} = \text{To be calculated later} \end{aligned} \tag{20}$$

Equations

$$\begin{aligned} C1+C2+C3 &= k1 \\ T2\bullet(C1+C3)+R3\bullet C3\bullet(C1+C2) &= k2 \\ R3\bullet C1\bullet C3 &= k3 \\ \frac{C3}{C1} &= k4\ (To\ be\ specified\ later) \end{aligned} \tag{21}$$

$$C1\bullet(k4+1)+C2=k1$$

$$T2\bullet C1\bullet(k4+1)+k3+\frac{k3\bullet C2}{C1}=k2 \tag{22}$$

Combining these leads to a quadratic equation that can be calculated ***C1***

$$T2\bullet(k4+1)\bullet C1^2-(k2+k3\bullet k4)\bullet C1+k3\bullet k1=0 \tag{23}$$

Determining the proper value for k4

Note that the larger ***k4*** is chosen, the larger ***C3*** will be, and this will be assumed to be desirable. This section shows how to compute the largest possible value for ***k4***.

The discriminant for equation (21) is:

$$A\bullet k4^2+B\bullet k4+C \tag{24}$$

Where

$$\begin{aligned} A &= k3^2 \\ B &= 2\bullet k2\bullet k3-4\bullet T2\bullet k3\bullet k1 \\ C &= k2^2-4\bullet T2\bullet k3\bullet k1 \end{aligned} \tag{25}$$

By setting the discriminant equal to zero and solving for ***k4***, one will get the restriction (***r1*** and ***r2*** are the roots, and ***r1*** < ***r2***):

$$\begin{aligned} &k4<r1 \\ &or \\ &k4>r2 \end{aligned} \tag{26}$$

From trial and error, it usually turns out that ***k4 = r1*** is the largest possible choice for ***k4*** that will yield component values that are both real and non-negative. Once ***k4*** is selected, equation (23) can be solved for ***C1***. Once ***C1*** is known, then ***C1***, ***C2***, ***R2***, and ***R3*** can be found in that order by applying equations (21) and (22). If the component values come out to be complex or negative, it may be necessary to adjust ***k4*** or ***T31***.

Conclusion

This chapter has presented two approaches to a third order passive loop filter design. The standard method uses some approximations to solve approximately for the component values in closed form. The exact uses no approximations, but requires numerical methods and more intense calculations. It is more work, but allows the user to specify the filter parameters without any approximations, and relaxes certain restrictions, such as the constraint that ***C3>C1/5***. Computer programs, such as Mathcad, make the exact approach much more practical and easier to implement. One unexpected result from simulations show that in the majority of cases, filters

calculated with the standard method actually have faster lock times than those calculated with the exact method. The reason for this is that maximizing the phase margin at the loop bandwidth is only an approximation for making the loop filter optimum in the sense of lock time.

Regardless of the filter calculation method used, the VCO input capacitance adds to capacitor ***C3***, so this component should be at least four times the VCO input capacitance. In many circumstances, this is not possible. If the value of ***T31*** is decreased, then the capacitor ***C3*** will become larger. Choosing ***C3*** as large as possible also corresponds to choosing ***R3*** as small as possible. It is desirable to not have the ***R3*** resistor too large, or else the thermal noise from this resistor can add to the out of band phase noise.

References

[1] Keese, William O. *An Analysis and Performance Evaluation of a Passive Filter Design Technique for Charge Pump Phased Locked Loops*

A THIRD ORDER LOOP FILTER DESIGN

USER NEEDS TO ENTER THESE :

$\phi := 50\,deg$ Phase margin

$Fc := 10\,kHz$ Loop Bandwidth

$Fcomp := 200\,kHz$ Comparison Frequency

$Kvco := 20\,\frac{MHz}{volt}$ VCO Gain

$K\phi := 5\cdot mA$ Phase Detector Pump Gain

$Fout := 2450\,MHz$ RF output frequency

$T31 := 0.80$ Ratio of Poles T3/T1. Choose between 0 and 1.

BASIC CALCULATIONS

$$N := \frac{Fout}{Fcomp} \qquad \omega c := 2\cdot\pi\cdot Fc$$

CALCULATIONS USING THE STANDARD METHOD

CALCLUATE POLES AND ZERO

$$T1 := \frac{\left(\frac{1}{\cos(\phi)}\right) - \tan(\phi)}{\omega c\cdot(T31 + 1)} \qquad T3 := T31\cdot T1 \qquad T2 := \frac{1}{(\omega c^2\cdot(T1 + T3))}$$

$T1 = 3.2186\cdot10^{-6}\,sec$ $T2 = 4.3795\cdot10^{-5}\,sec$ $T3 = 2.5751\cdot10^{-6}\,sec$

CALCULATE COMPONENTS FROM POLES AND ZERO

$$Ctot := \frac{K\phi\cdot Kvco}{\omega c^2\cdot N}\cdot\left[\frac{1 + \omega c^2\cdot T2^2}{(1 + \omega c^2\cdot T1^2)\cdot(1 + \omega c^2\cdot T3^2)}\right]^{\frac{1}{2}} \qquad C1 := Ctot\frac{T1}{T2}$$

$$C3 := \frac{C1}{5} \qquad C2 := Ctot - C1 - C3$$

$$R2 := \frac{T2}{C2} \qquad R3 := \frac{T3}{C3}$$

DISPLAY COMPONENT VALUES

$C1 = 430.5273\,pF$ $C2 = 5.3331\,nF$ $C3 = 86.1054\,pF$

$R2 = 8.1991\,k\Omega$ $R3 = 29.9001\,\Omega$

LOOP FILTER ANALYSIS FOR THE STANDARD METHOD

CALCULATE TRUE POLES AND ZERO

$T2 := R2 \cdot C2$

$$x := \frac{C2 \cdot C3 \cdot R2 + C1 \cdot C2 \cdot R2 + C1 \cdot C3 \cdot R3 + C2 \cdot C3 \cdot R3}{C1 + C2 + C3}$$ This is T1+T3

$$y := \frac{R2 \cdot R3 \cdot C1 \cdot C2 \cdot C3}{C1 + C2 + C3}$$ This is T1*T3

$$T1 := \frac{x + \sqrt{x^2 - 4 \cdot y}}{2} \qquad T3 := \frac{x - \sqrt{x^2 - 4 \cdot y}}{2}$$

Time Constant	Filter Pole	Filter Zero
$T1 = 4.596 \cdot 10^{-6}\ sec$	$\frac{1}{T1} = 217.6\ kHz$	n/a
$T2 = 4.378 \cdot 10^{-5}\ sec$	n/a	$\frac{1}{T2} = 22.86\ kHz$
$T3 = 1.804 \cdot 10^{-6}\ sec$	$\frac{1}{T3} = 554.65\ kHz$	n/a

$\frac{T3}{T1} = 39.23\ \%$

DEFINE LOOP PARAMETERS

$$Z(\omega) := \frac{1 + T2 \cdot i \cdot \omega}{i \cdot \omega \cdot (C1 + C2 + C3) \cdot (1 + i \cdot \omega \cdot T1) \cdot (1 + i \cdot \omega \cdot T3)}$$ Loop Filter Impedance

$$G(\omega) := \frac{K\phi \cdot Kvco \cdot Z(\omega)}{i \cdot \omega}$$ Forward Loop Gain

LOOP BANDWIDTH AND PHASE MARGIN

$\omega := 10.0\ kHz$

$\omega c := root(|G(\omega)| - N, \omega)$ $\frac{\omega c}{2 \cdot \pi} = 9.889\ kHz$ Loop Bandwidth

$\omega := \omega c$

$arg(G(\omega c)) \cdot \frac{180}{\pi} + 180 = 47.465$ Phase Margin

CALCULATIONS USING THE EXACT METHOD

CALCULATE THE POLES AND ZERO $\omega c := 2 \cdot \pi \cdot Fc$

Solve for T1 and T2

$$f(x) := \frac{x}{1 + x^2} + \frac{x \cdot T31}{1 + (x \cdot T31)^2} \qquad g(x) := \frac{1 + \sqrt{1 - 4 \cdot f(x)^2}}{2 \cdot f(x)}$$

This finds wcT2 as a function of wcT1 (or x)

$x := 3 \cdot 10^{-5}$

$$T1 := \frac{root(\phi - atan(g(x)) + atan(x) + atan(x \cdot T31), x)}{\omega c}$$

$$T2 := \frac{g(\omega c \cdot T1)}{\omega c} \qquad T3 := T31 \cdot T1$$

$T1 = 3.011 \cdot 10^{-6} \cdot sec$ $T2 = 4.215 \cdot 10^{-5} \cdot sec$ $T3 = 2.406 \cdot 10^{-6} \cdot sec$

CALCULATE COMPONENTS FROM POLES AND ZERO

Set Up System of 4 equations and 4 unknowns

$$k1 := \left(\frac{K\phi \cdot Kvco}{N}\right) \cdot \sqrt{\frac{1 + (\omega c \cdot T2)^2}{(1 + (\omega c \cdot T1)^2) \cdot (1 + (\omega c \cdot T3)^2)}} \cdot \frac{1}{\omega c^2} \qquad k1 = 5.687\,nF$$

$k2 := (T1 + T3) \cdot k1$ $k2 = 3.084 \cdot 10^{-5} \cdot sec \cdot nF$

$$k3 := \frac{T3 \cdot T1 \cdot k1}{T2} \qquad k3 = 9.779 \cdot 10^{-7} \cdot sec \cdot nF$$

Use these equations to find a maximum value for k4

$A := k3^2$ $A = 9.562 \cdot 10^{-13} \cdot sec^2 \cdot nF^2$

$B := 2 \cdot k2 \cdot k3 - 4 \cdot T2 \cdot k1 \cdot k3$ $B = -8.772 \cdot 10^{-10} \cdot sec^2 \cdot nF^2$

$C := k2^2 - 4 \cdot T2 \cdot k3 \cdot k1$ $C = 1.172 \cdot 10^{-11} \cdot sec^2 \cdot nF^2$

$$k4min := \frac{-B - \sqrt{B^2 - 4 \cdot A \cdot C}}{2 \cdot A} \qquad k4min = 0.013$$

$$k4max := \frac{-B + \sqrt{B^2 - 4 \cdot A \cdot C}}{2 \cdot A} \qquad k4max = 917.355 \qquad k4 := k4min$$

Solve for C1 and other Components

$A := T2 \cdot (k4 + 1)$

$B := -k2 - k3 \cdot k4$

$C := k3 \cdot k1$

$C1 := \frac{-B}{2 \cdot A}$

$C2 := k1 - C3 - C1$

$A = 4.271 \cdot 10^{-5} \cdot \text{sec}$

$B = -0.031 \cdot \text{sec} \cdot \text{pF}$

$C = 5.561 \cdot \text{sec} \cdot \text{pF}^2$

$C3 := k4 \cdot C1$

$R3 := \frac{k3}{C1 \cdot C3}$ $R2 := \frac{T2}{C2}$

DISPLAY COMPONENT VALUES

$C1 = 360.827239 \cdot \text{pF}$ $C2 = 5.320894 \cdot \text{nF}$ $C3 = 4.820217 \cdot \text{nF}$

$R2 = 7.920958 \cdot \text{k}\Omega$ $R3 = 562.22499 \cdot \text{k}\Omega$

LOOP FILTER ANALYSIS FOR THE EXACT METHOD

CALCULATE TRUE POLES AND ZERO

$T2 := R2 \cdot C2$

$x := \frac{C2 \cdot C3 \cdot R2 + C1 \cdot C2 \cdot R2 + C1 \cdot C3 \cdot R3 + C2 \cdot C3 \cdot R3}{C1 + C2 + C3}$ This is T1+T3

$y := \frac{R2 \cdot R3 \cdot C1 \cdot C2 \cdot C3}{C1 + C2 + C3}$ This is T1*T3

$T1 := \frac{x + \sqrt{x^2 - 4 \cdot y}}{2}$ $T3 := \frac{x - \sqrt{x^2 - 4 \cdot y}}{2}$

Time Constant	Filter Pole	Filter Zero
$T1 = 3.011 \cdot 10^{-6} \cdot sec$	$\frac{1}{T1} = 332.238 \cdot kHz$	n/a
$T2 = 4.215 \cdot 10^{-5} \cdot sec$	n/a	$\frac{1}{T2} = 23.721 \cdot kHz$
$T3 = 2.408 \cdot 10^{-6} \cdot sec$	$\frac{1}{T3} = 415.298 \cdot kHz$	n/a

$\frac{T3}{T1} = 80 \cdot \%$

DEFINE LOOP PARAMETERS

$Z(\omega) := \frac{1 + T2 \cdot i \cdot \omega}{i \cdot \omega \cdot (C1 + C2 + C3) \cdot (1 + i \cdot \omega \cdot T1) \cdot (1 + i \cdot \omega \cdot T3)}$ Loop Filter Impedance

$G(\omega) := \frac{K\phi \cdot Kvco \cdot Z(\omega)}{i \cdot \omega}$ Forward Loop Gain

LOOP BANDWIDTH AND PHASE MARGIN

$\omega := 10.0 \cdot kHz$

$\omega c := root(|G(\omega)| - N, \omega)$ $\frac{\omega c}{2 \cdot \pi} = 10 \cdot kHz$ Loop Bandwidth

$\omega := \omega c$

$arg(G(\omega c)) \cdot \frac{180}{\pi} + 180 = 50$ Phase Margin

10. Fourth and Higher Order Passive Loop Filter Designs

Introduction

The order of a PLL system is defined as one plus the number of poles in the loop filter. This chapter investigates the design of filters of fourth and higher order loop filters. The motivation for doing higher order filter designs is reduced spur levels. Fourth order and higher order filters become more practical when the spur to be filtered is at least 20 times the loop bandwidth. Although this chapter investigates the general case for the higher order filters, the fourth order will be used for most of the examples and diagrams. Equations for filter orders higher than four are more of an academic exercise than something of practical value.

In the case of a fourth order filter, it is not any more difficult to solve for the time constants exactly than it is for the third order filter. However, an exact solution of the components from the time constants is very difficult and beyond the scope of this book. As in the third order filter, either the standard or exact method can be used to calculate the time constants, but approximations will be introduced to solve for the components. To solve for the components, both a standard method and a high precision method will be given. The high precision method works provided $T41 < 2 \bullet T31$. For the four order filter, the user needs to specify the loop bandwidth, wc, phase margin, f, pole ratio $T31$, and pole ratio $T41$.

Circuit Topology

A fourth order loop filter is shown below. Higher order loop filters are possible by adding additional RC filters. Buffers can be put between the stages to improve the isolation.

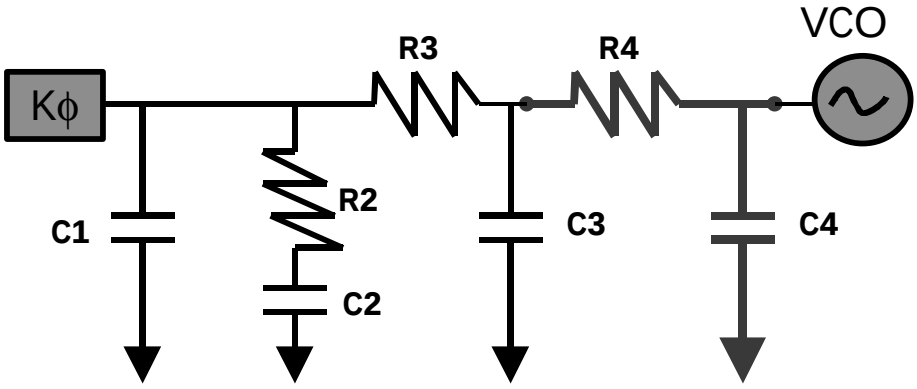


Figure 1 *Fourth Order Passive Filter*

Loop Filter Impedance and Time Constant Derivation

The loop filter impedance for the fourth order loop filter is given below:

$$Z(s) = \frac{1 + s \bullet C2 \bullet R2}{s \bullet (A \bullet s^3 + B \bullet s^2 + C \bullet s + D)} = \frac{1 + s \bullet T2}{s \bullet Ctot \bullet (1 + s \bullet T1) \bullet (1 + s \bullet T3) \bullet (1 + s \bullet T4)} \quad (1)$$

where

$$Ctot = C1+C2+C3+C4$$

$$T2 = R2 \bullet C2 \qquad (2)$$
$$A = C1 \bullet C2 \bullet C3 \bullet C4 \bullet R2 \bullet R3 \bullet R4$$
$$B = C1 \bullet C2 \bullet R2 \bullet R3 \bullet (C3+C4) + R4 \bullet C4 \bullet (C2 \bullet C3 \bullet R3 + C1 \bullet C3 \bullet R3 + C1 \bullet C2 \bullet R2)$$
$$C = C2 \bullet R2 \bullet (C1+C3+C4) + R3 \bullet (C1+C2) \bullet (C3+C4) + R4 \bullet C4 \bullet (C1+C2+C3)$$
$$D = Ctot$$
$$T1 = \frac{R2 \bullet C2 \bullet C1}{Ctot}$$
$$T3 \approx R3 \bullet C3$$
$$T4 \approx R4 \bullet C4$$

For the general k[th] order loop filter, the impedance and time constants are:

$$Z(s) = \frac{(1 + s \bullet T2)}{s \bullet Ctot \bullet (1 + s \bullet T1) \bullet \prod_{i=3}^{k} (1 + s \bullet T_i)} \qquad (3)$$

where

$$\begin{aligned} T1 &\approx R2 \bullet C2 \bullet \frac{C1}{Ctot} \\ T2 &= R2 \bullet C2 \\ T_i &= R_i \bullet C_i \qquad\qquad i = 3,4, \ldots k \end{aligned} \qquad (4)$$

Now the equations shown above are reasonably good approximations, although the time constants of the loop filter have been approximated. These approximation holds true as long as:

$$C_i << C1 \qquad (5)$$

$$1 << \left(\frac{C_i}{C_{i+1}}\right) + \left(\frac{R_{i+1}}{R_i}\right) \qquad i=3,4,..k \qquad (6)$$

One possible way to ensure that the above constraints are satisfied is to choose:

$$T_i \geq 2 \bullet T_{i+1} \qquad (7)$$

Solving for the Time Constants

In a similar way is calculated for a third order filter, the phase margin is given by:

$$f = 180 + \tan^{-1}(wc \bullet T2) - \tan^{-1}(wc \bullet T1) - \prod_{i=3}^{k} \tan^{-1}(wc \bullet T_i) \qquad (8)$$

From the Taylor Series, for small x it can be shown:

$$\begin{aligned} \tan(x) &\approx x \\ \tan^{-1}(x) &\approx x \end{aligned} \qquad (9)$$

Applying the ***tan*** function and the two previous identities yields the following simplification:

$$T1 + \sum_{i=3}^{k} T_i \approx \frac{sec(f) - tan(f)}{wc} \tag{10}$$

As a design constraint the phase margin is maximized at the loop bandwidth. Setting the derivative of the phase margin equal to zero yields the following equation

$$\frac{T2}{1 + wc^2 \bullet T2^2} = \frac{T1}{1 + wc^2 \bullet T1^2} + \sum_{i=3}^{k} \frac{T_i}{1 + wc^2 \bullet T_i^2} \tag{11}$$

Cross multiplying both sides and applying some approximations yields:

$$T2 \approx wc^2 \bullet T2^2 \bullet (T1 + \sum_{i=3}^{k} T_i) \tag{12}$$

Now a great many number of terms have been eliminated, and this simplification can be justified as long as:

$$T2 >> T1 + \sum_{i=3}^{k} T_i \tag{13}$$

Rearranging equation (12) yields the following:

$$T2 \approx \frac{1}{wc^2 \bullet (T1 + \sum_{i=3}^{k} T_i)} \tag{14}$$

$$T1 + \sum_{i=3}^{n} T_i \frac{sec(f) - tan(f)}{wc} \tag{15}$$

Now the choice of the time constants $T1$, T_3, ... T_k can all be chosen equal for optimal spurious attenuation, or can be chosen as in (7) to avoid too much error due to mathematical approximations. In the case of a 4th order filter, to satisfy (7) choose:

$$T1 = \frac{4}{7} \bullet \frac{sec(f) - tan(f)}{wc}$$

$$T_3 \equiv T3 = \frac{2}{7} \bullet \frac{sec(f) - tan(f)}{wc}$$

$$T_4 \equiv T4 = \frac{1}{7} \bullet \frac{sec(f) - tan(f)}{wc}$$

Solving for the Components from the Time Constants
Once these time constants are known, the other components can be calculated

$$Ctot = \frac{Kf \bullet Kvco}{wc^2 \bullet N} \bullet \sqrt{\frac{1 + wc^2 \bullet T2^2}{(1 + wc^2 \bullet T1^2) \bullet \prod_{i=3}^{k} (1 + wc^2 \bullet T_i^2)}}$$

$$C1 = Ctot \bullet \frac{T1}{T2}$$

$$C3 = \frac{C1}{5}$$

$$C4 = \frac{C3}{5}$$

$$C_{i+1} = \frac{C_i}{5} \quad i = 4,5,6,... \quad \text{(zero if the filter order is four or less)}$$

$$C2 = Ctot - C1 - C3 - C4 - \sum_{i=5,6,7,...} C_i$$

$$R2 = \frac{T2}{C2}$$

$$R3 = \frac{T3}{C3}$$

$$R4 = \frac{T4}{C4}$$

$$R_i = \frac{T_i}{C_i} \quad i = 4,5,6... \quad \text{(zero if the filter order is four or less)}$$

An Improvement in Component Calculations for the Fourth Order Filter

In the case of a fourth order filter, the components can be calculated more precisely by writing explicitly the impedance for the components ***R3***, ***R4***, ***C3***, and ***C4*** and solving for the time constants T3 and T4 more exactly. This approximation is very similar to putting an op-amp right before R3, except for the time constant T1 still takes into account the loading from the rest of the components of the loop filter.

The components ***C1***, ***C2***, ***C3***, and ***R2*** are calculated as normal, however, the components ***R3***, ***R4***, and ***C4*** are found more exactly by equating the poles to the expressing for the loop filter impedance. The voltage transfer function from the beginning of resistor ***R3*** to the input of the VCO is:

$$\frac{1}{1 + s \bullet (C3 \bullet R3 + C4 \bullet R4 + R3 \bullet C4) + s^2 \bullet C3 \bullet C4 \bullet R3 \bullet R4} = \frac{1}{(1 + s \bullet T3) \bullet (1 + s \bullet T4)}$$

Doing this arithmetic yields the values for ***R3*** and ***R4***.

$$R3, R4 = \frac{T3 + T4 \mp \sqrt{(T3 + T4)^2 - 4 \bullet T3 \bullet T4 \bullet \left(1 + \frac{C4}{C3}\right)}}{2 \bullet (C3 + C4)}$$

For real component values, the quantity under the square root sign must be non-negative. Applying this restriction yields:.

$$\frac{C4}{C3} \le \frac{(T3-T4)^2}{4 \bullet T3 \bullet T4}$$

However, it is desirable to choose C4 as large as possible, so this quantity should be made equal. ***T3*** should be chosen larger than ***T4***, (ie. ***T31*** > ***T41***) so that the capacitor ***C3*** is non-zero and that it is at least three times the VCO input capacitance. Applying this restriction yields the component values:

$$C4 = C3 \bullet \frac{(T3-T4)^2}{4 \bullet T3 \bullet T4}$$

$$R3 = R4 = \frac{T3+T4}{2 \bullet (C3+C4)}$$

Conclusion

The design and simulation of a fourth order filter has been presented. The fourth order filter provides the most benefit in situations where the offset frequency of the spurs is at least 20 times the loop bandwidth. These concepts can be applied also to fifth, sixth, and higher order filters. Higher order filters often become unrealistic because the required capacitor values become too small relative to the VCO input capacitance and they become unnecessarily complex. In future chapters, the benefit of using filter of higher than second order will be examined in depth.

References

[1] Keese, William O. *An Analysis and Performance Evaluation of a Passive Filter Design Technique for Charge Pump Phased Locked Loops*

A FOURTH ORDER LOOP FILTER DESIGN

USER NEEDS TO ENTER THESE

$Kvco := 20\frac{MHz}{volt}$ VCO Gain

$K\phi := 5 \cdot mA$ Charge Pump Gain

$Fout := 900MHz$ RF output frequency

$Fcomp := 1000kHz$ Comparison Frequency

$Fc := 10kHz$ Loop Bandwidth

$\phi := 50deg$ Phase margin. Default is 50 degrees.

$T31 := 1.0$ Ratio of the Pole T3 to T1. Enter 0 to 1.

$T41 := 0.5$ Ratio of the Pole T4 to the Pole T3. Enter 0 to 1.

CALCULATIONS

$N := \frac{Fout}{Fcomp}$ $\omega c := 2 \cdot \pi \cdot Fc$

CALCULATE POLES AND ZERO

$$T1 := \frac{\left(\frac{1}{\cos(\phi)} - \tan(\phi)\right)}{\omega c} \cdot \frac{1}{1 + T31 + T41}$$

$T3 := T1 \cdot T31$ $T4 := T41 \cdot T1$ $T2 := \frac{1}{(\omega c^2 \cdot (T1 + T3 + T4))}$

$T1 = 2.317 \cdot 10^{-6} sec$ $T2 = 4.379 \cdot 10^{-5} sec$ $T3 = 2.317 \cdot 10^{-6} sec$ $T4 = 1.159 \cdot 10^{-6} sec$

CALCULATE COMPONENT VALUES FROM TIME CONSTANTS

$$Ctot := \frac{K\phi \cdot Kvco}{\omega c^2 \cdot N} \cdot \left[\frac{1 + \omega c^2 \cdot T2^2}{(1 + \omega c^2 \cdot T1^2) \cdot (1 + \omega c^2 \cdot T3^2) \cdot (1 + \omega c^2 \cdot T4^2)} \right]^{\frac{1}{2}}$$

$$C1 := Ctot \frac{T1}{T2} \qquad C3 := \frac{C1}{5} \qquad C4 := C3 \cdot \frac{(T3 - T4)^2}{4 \cdot T3 \cdot T4}$$

$$C2 := Ctot - C1 - C3 - C4 \qquad R2 := \frac{T2}{C2}$$

$$R3 := \frac{T4 + T3}{2 \cdot (C3 + C4)} \qquad R4 := \frac{T4 + T3}{2 \cdot (C3 + C4)}$$

CALCULATED VALUES:

$C1 = 4.259 \cdot 10^{3}\ pF$ $C2 = 7.515 \cdot 10^{4}\ pF$ $C3 = 851.748\ pF$ $R2 = 0.582\ k\Omega$ $R3 = 1.814\ k\Omega$

$C4 = 106.468\ pF$ $R4 = 1.814\ k\Omega$

SIMULATION

DEFINE LOOP PARAMETERS

$$A := R2 \cdot R3 \cdot R4 \cdot C1 \cdot C2 \cdot C3 \cdot C4$$

$$B := C1 \cdot C2 \cdot R2 \cdot R3 \cdot (C3 + C4) + R4 \cdot C4 \cdot (C2 \cdot C3 \cdot R3 + C1 \cdot C3 \cdot R3 + C1 \cdot C2 \cdot R2)$$

$$C := R2 \cdot C2 \cdot (C1 + C3 + C4) + R3 \cdot (C1 + C2) \cdot (C3 + C4) + R4 \cdot C4 \cdot (C1 + C2 + C3)$$

$$D := C1 + C2 + C3 + C4$$

$$Z(s) := \frac{1 + s \cdot C2 \cdot R2}{s \cdot (A \cdot s^3 + B \cdot s^2 + C \cdot s + D)} \qquad G(\omega) := \frac{K\phi \cdot Kvco \cdot Z(\omega \cdot i)}{\omega \cdot i}$$

$$\omega := 10\,kHz$$

$$\omega c := root(|G(\omega)| - N, \omega) \qquad \frac{\omega c}{2 \cdot \pi} = 9.987\,kHz$$

$$\phi := arg(G(\omega c)) \cdot \frac{180}{\pi} + 180 \qquad \phi = 53.093$$

11. Fundamentals of PLL Active Loop Filter Design

Introduction

The following several chapters have discussed passive loop filter designs. Passive loop filters are generally recommended over active filters for reasons of cost, simplicity, and in-band phase noise. The added in-band phase noise comes from the active device that is used in the loop filter. However, in cases where the VCO requires a higher tuning voltage than the PLL charge pump can operate, active filters are necessary. VCOs with high voltage tuning requirements are most common in broadband tuning applications, such as those encountered in cable TV tuners. It is also commonly required for low noise or high power VCOs.

With older styles of phase detectors, before the charge pump PLL, active filters were used in order to obtain a zero steady-state phase error and infinite pull-in range. However, this is not a good reason to use an active filter with a charge pump PLL, since the charge pump PLL always attains these characteristics with a passive filter.

Many of the concepts presented in this chapter are analogous to those in passive loop filter design. The solution for the time constants is identical, however the solution of components from those time constants is not the same, since the active device does provide isolation for the higher stages. The concepts for loop bandwidth, phase margin and pole ratios all apply. However, it is generally recommended to use at least a third order filter, since the added pole reduces the phase noise of the active device.

Types of Active Filters

The two basic classes of active filters are those using the differential charge pump outputs and those which use the charge pump output pin. For each of these two basic classes, there are also different variations for the loop filter topology. Since most of the concepts in this chapter are not applicable to the approach involving the differential phase detector outputs, this case is treated in a separate chapter.

The other approaches presented all involve using active devices to boost the charge pump output voltage. One such way involves simply adding a gain stage before the VCO. Other approaches involve putting components in the feedback path of the active loop filter device.

Regardless of the approach used, there is an inversion introduced, which can be negated by reversing the polarity of the charge pump. There is also isolation added, which allows a larger capacitor to be chosen next to the VCO to reduce the impact of the VCO input capacitance and loop filter resistor noise.

The Three Approaches of Charge Pump Active Filters
Simple Gain Approach

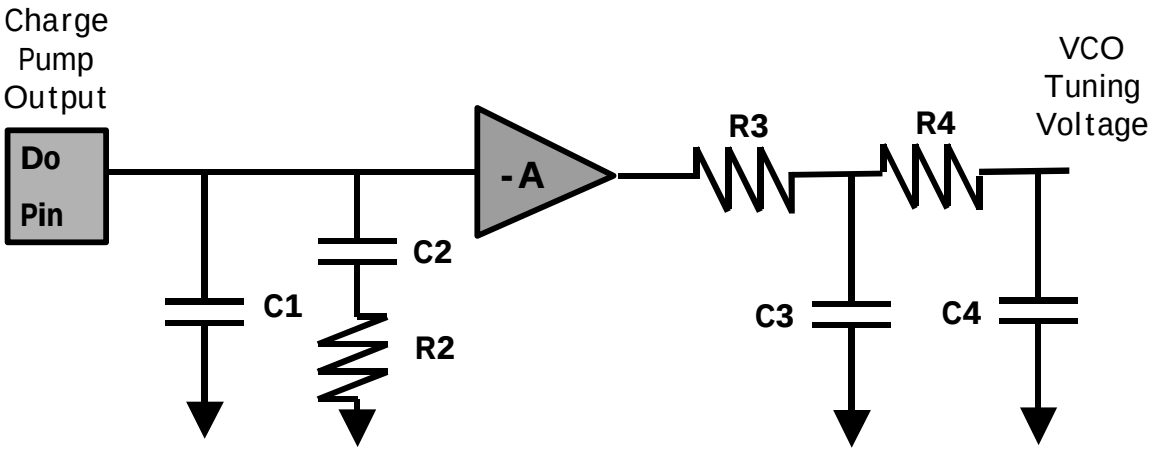


Figure 1a *An Active Filter Using the Simple Gain Approach*

This approach involves placing an op-amp in front of the VCO. The advantage of this approach is that it is very intuitive and commonly used. Since the op-amp generates noise, it is generally recommended to use a third or higher order filter to reduce the op-amp noise, even if the spurs do not benefit much from it.

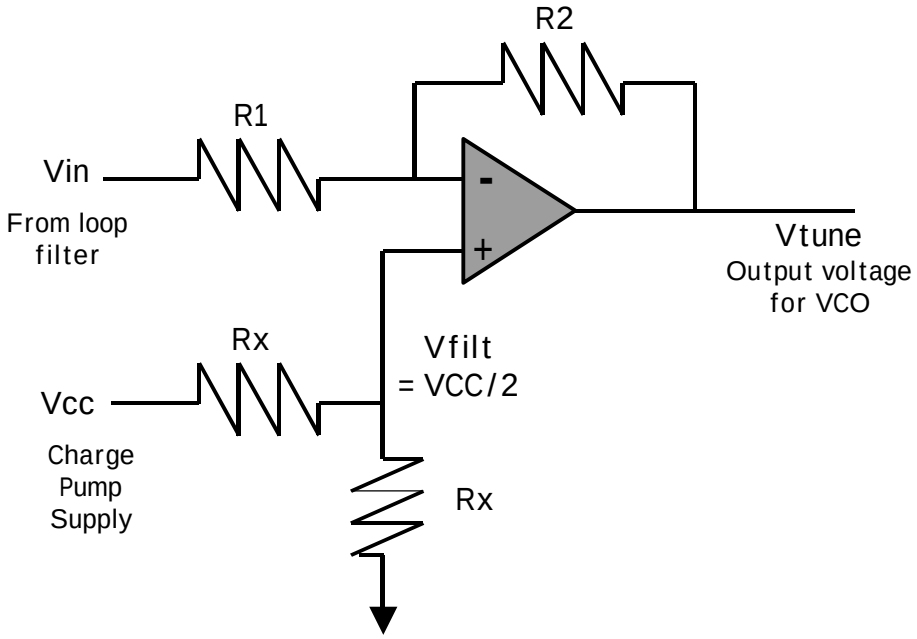


Figure 1b *Op-amp Configuration which Produces Gain –**A** Centered at Vcc/2*

The gain of ***–A*** is produced by using an op-amp in an inverting configuration. The resistor ***Rx*** is selected to be large enough so that the current consumption is not excessive. However, choosing ***Rx*** excessively large could lead to problems due to the resistor thermal noise.

Standard Feedback Approach

This approach involves putting the components ***C1***, ***C2***, and ***R2*** in the feedback path of an op-amp. Additional filtering stages are added after the op-amp. This approach is generally superior to the simple gain approach because it allows the charge pump voltage to be centered at half the charge pump supply, for lower and more predictable spur levels.

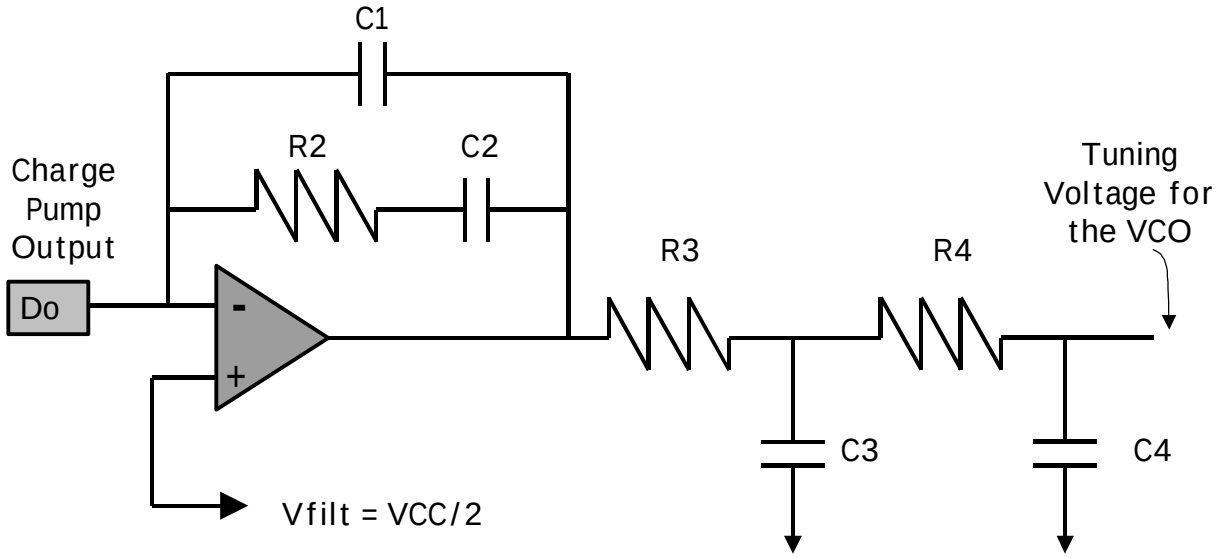


Figure 2 *An Active Filter Using the Standard Feedback Approach*

Alternative Feedback Approach

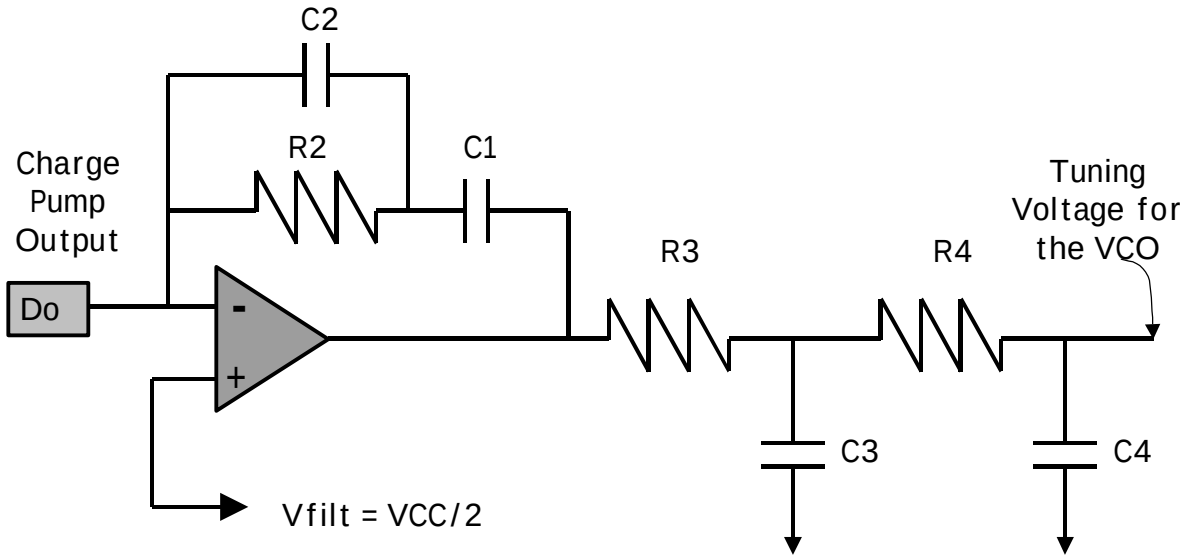


Figure 3 *An Active Filter Using the Alternative Feedback Approach*

This approach is very similar to the standard feedback approach, except that the topology is slightly changed. The only possible advantages or disadvantages of this approach would be a consequence of the fact that the actual calculated component values will be different.

Using Transistors for the Standard and Alternative Feedback Approaches

For either of the feedback approaches, transistors can be used to replace the op-amp in order to reduce the cost and the noise. For the approach presented here, the transistors can only sink current, so a pull-up resistor, ***Rpp***, is required. The choice of ***Rpp*** is design and possibly transistor specific, but ***Rpp = 10 KW*** is a good starting value. Choosing this resistor too large will cause the circuit to be unstable and the carrier to dance around the frequency spectrum. Choosing it too small will cause excessive current consumption since ***Vpp*** is grounded through the resistor ***Rpp*** when the transistors turn on. This particular design has been built and tested to 30 volt operation. The optional 20 KΩ resistor may reduce the phase noise.

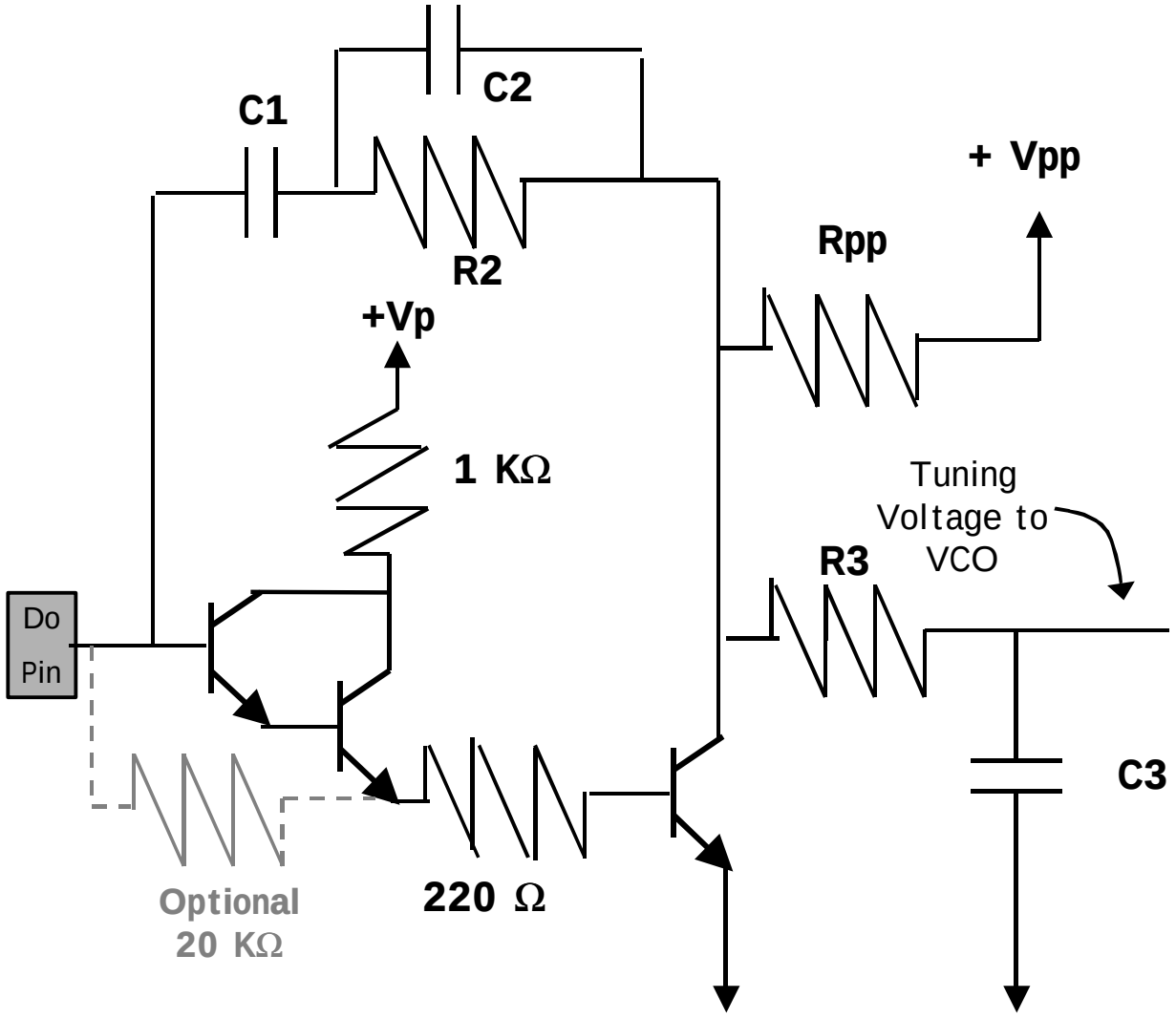


Figure 4 *Third Order Alternative Feedback Active Filter Using Transistors*

Loop Filter Impedance and Forward Loop Gain

The loop filter impedance is defined as the output voltage to the VCO generated by a current produced from the charge pump. Regardless of the approach used, the loop filter impedance can be expressed in the following form:

$$Z(s)=\frac{1+s\bullet T2}{s\bullet Cx}\bullet\frac{-A}{(1+s\bullet T1)\bullet(1+s\bullet T3)\bullet(1+s\bullet T4)}$$

Assuming that the charge pump polarity is inverted, the open loop gain becomes:

$$G(s)/N=-\frac{Kf\bullet Kvco\bullet A}{w^2\bullet N}\bullet\frac{1+s\bullet T2}{s\bullet Cx\bullet(1+s\bullet T1)\bullet(1+s\bullet T3)\bullet(1+s\bullet T4)}$$

	Simple Gain Approach	Standard Feedback Approach	Alternative Feedback Approach
T1	$\frac{C1\bullet C2\bullet R2}{C1+C2}$	$\frac{C1\bullet C2\bullet R2}{C1+C2}$	$C2\bullet R2$
T2	$C2\bullet R2$	$C2\bullet R2$	$R2\bullet(C1+C2)$
T3	$\frac{(C3\bullet R3+C4\bullet R3+C4\bullet R4)+\sqrt{(C3\bullet R3+C4\bullet R3+C4\bullet R4)^2-4\bullet C3\bullet C4\bullet R3\bullet R4}}{2}$		
T4	$\frac{(C3\bullet R3+C4\bullet R3+C4\bullet R4)-\sqrt{(C3\bullet R3+C4\bullet R3+C4\bullet R4)^2-4\bullet C3\bullet C4\bullet R3\bullet R4}}{2}$		
Cx	$C1+C2$	$C1+C2$	$C1$
A	*Set by op-amp Configuration*	1	1

Table 1 *Filter Parameters as they Relate to the Filter Components*

Calculating the Loop Filter Components

Solving for the time constants

The first step in calculating the loop filter components is calculating the time constants. This is done in exactly the same way that it was done in the case of a passive filter, and is therefore not shown again in this chapter. Once the time constants are known, the loop filter components can be calculated from these time constants.

Solving for Cx

The first step in solving for the components is determining the value of ***Cx***. This can be found by setting the open loop gain equal to one at the loop bandwidth.

$$Cx=\frac{Kf\bullet Kvco\bullet A}{wc^2\bullet N}\bullet\sqrt{\frac{1+wc^2\bullet T2}{(1+wc^2\bullet T1)\bullet(1+wc^2\bullet T3)\bullet(1+wc^2\bullet T4)}}$$

Solving for the Components

Once that ***Cx*** is found, the other components can be found using the Table 2. For a third order loop filter, ***C3*** should be at least four times the VCO input capacitance and at least ***C1/5***. For a fourth order loop filter, ***C4*** should be at least this stated limit above.

	Simple Gain Approach	Standard Feedback Approach	Alternative Feedback Approach
C1	$Cx \bullet \frac{T1}{T2}$	$Cx \bullet \frac{T1}{T2}$	Cx
C2	$Cx \bullet \left(1 - \frac{T1}{T2}\right)$	$Cx \bullet \left(1 - \frac{T1}{T2}\right)$	$Cx \bullet \frac{T1}{T2 - T1}$
R2	$\frac{T2}{C2}$	$\frac{T2}{C2}$	$\frac{T2}{C1 + C2}$
Third Order Filter Components			
C3	*Choose C3 at least 4X the VCO input capacitance and at least 200 pF.*		
R3	$\frac{T3}{C3}$		
Fourth Order Components			
C4	*Choose C4 at least 4X the VCO input capacitance and preferably at least 200 pF. Also make sure that this yields realistic values for C3.*		
C3	$C4 \bullet \frac{4 \bullet T3 \bullet T4}{(T3 - T4)^2}$		
R3	$\frac{T3 + T4}{2 \bullet (C3 + C4)}$		
R4	$\frac{T3 + T4}{2 \bullet (C3 + C4)}$		

Table 2 *Loop Filter Component Values Computed from Time Constants*

Conclusion

The equations for active loop filter design have been presented. Active filters are necessary when the charge pump can not operate at high enough voltages to tune the VCO. Active devices in the loop filter do introduce noise, but also allow larger capacitor values to be placed next to the VCO in order to reduce the impact of the VCO input capacitance and loop filter resistor thermal noise.

Very little was said in this chapter on how to pick an op-amp that is suitable for the loop filter, but this choice is important. The offset voltage is irrelevant, but the voltage noise should be very low. A poor choice for the op-amp could easily increase the phase noise by 10 dB, while a good choice would probably increase the phase noise by a couple dB. Some popular choices are the OP27 and the LMX6132/42. The bandwidth of the op-amp is not very critical, but it could have some minor impact on phase noise and lock time. It should be higher than the natural ringing frequency of the PLL, so that it will not impact lock time. However, a narrower bandwidth of the op-amp may also help attenuate phase noise farther from the carrier.

FUNDAMENTALS OF ACTIVE FILTER DESIGN

USER NEEDS TO ENTER THESE

$Kvco := 44 \frac{MHz}{volt}$ VCO Gain

$K\phi := 5 \cdot mA$ Phase Detector Gain

$Fout := 2441 MHz$ RF output frequency

$Fcomp := 500 kHz$ Comparison Frequency

$Fc := 20 kHz$ Loop Bandwidth

$\phi := 50 deg$ Phase margin

$T31 := 0.5$ Ratio of poles T3 to T1

CALCULATIONS

$$N := \frac{Fout}{Fcomp} \qquad \omega c := 2 \cdot \pi \cdot Fc$$

$$T1 := \frac{\frac{1}{\cos(\phi)} - \tan(\phi)}{\omega c} \cdot \frac{1}{1 + T31} \qquad T3 := T1 \cdot T31$$

$$T2 := \frac{1}{(\omega c^2 \cdot (T1 + T3))}$$

DERIVED QUANTITIES

Parameters	Time Constants	Filter Poles	Filter Zero
	$T1 = 1.931 \cdot 10^{-6}\ sec$	$\frac{1}{T1 \cdot 2 \cdot \pi} = 82.424\ kHz$	$\frac{1}{T2 \cdot 2 \cdot \pi} = 7.279\ kHz$
$N = 4.882 \cdot 10^{3}$	$T2 = 2.186 \cdot 10^{-5}\ sec$		
	$T3 = 9.655 \cdot 10^{-7}\ sec$	$\frac{1}{T3 \cdot 2 \cdot \pi} = 164.848\ kHz$	

$$Cx := \frac{K\phi \cdot Kvco}{\omega c^2 \cdot N} \cdot \sqrt{\frac{1 + (\omega c \cdot T2)^2}{(1 + (\omega c \cdot T1)^2) \cdot (1 + (\omega c \cdot T3)^2)}}$$

STANDARD FEEDBACK APPROACH

$C1 := Cx \cdot \frac{T1}{T2}$ $C2 := Cx \cdot \left(1 - \frac{T1}{T2}\right)$ $C3 := 200pF$

$R2 := \frac{T2}{C2}$ $R3 := \frac{T3}{C3}$

COMPONENT VALUES

$C1 = 710.883pF$ $C2 = 7.338nF$ $C3 = 200pF$

$R2 = 2.979k\Omega$ $R3 = 4.824k\Omega$

DEFINE LOOP PARAMETERS

$Z(\omega) := \frac{1 + R2 \cdot C2 \cdot i \cdot \omega}{(1 + i \cdot \omega \cdot T1) \cdot (1 + i \cdot \omega \cdot T3) \cdot i \cdot \omega \cdot (C1 + C2)}$ Loop Filter Impedance

$G(\omega) := \frac{K\phi \cdot Kvco \cdot Z(\omega)}{i \cdot \omega}$ Forward Loop Gain

$CL(\omega) := \frac{G(\omega)}{1 + \frac{G(\omega)}{N}}$ Closed Loop Gain

BANDWIDTH AND PHASE MARGIN

$\omega := 10.0kHz$

$\omega c := root(|G(\omega)| - N, \omega)$ $\frac{\omega c}{2 \cdot \pi} = 20.0kHz$ Loop Bandwidth

$\frac{180}{\pi} \cdot arg(G(\omega c)) + 180 = 49.443$ Phase Margin

ALTERNATIVE FEEDBACK APPROACH

$C1 := Cx$ $\quad C2 := Cx \cdot \frac{T1}{T2 - T1}$ $\quad C3 := 200pF$

$R2 := \frac{T2}{C1 + C2}$ $\quad R3 := \frac{T3}{C3}$

COMPONENT VALUES

$C1 = 8.049 \cdot 10^{3}\,pF$ $\quad C2 = 0.78\,nF$ $\quad C3 = 200\,pF$

$R2 = 2.478\,k\Omega$ $\quad R3 = 4.824\,k\Omega$

DEFINE LOOP PARAMETERS

$$Z(\omega) := \frac{1 + i \cdot \omega \cdot R2 \cdot (C1 + C2)}{i \cdot \omega \cdot C1 \cdot (1 + i \cdot \omega \cdot C2 \cdot R2) \cdot (1 + i \cdot \omega \cdot R3 \cdot C3)}$$

Loop Filter Impedance

$$G(\omega) := \frac{K\phi \cdot Kvco \cdot Z(\omega)}{i \cdot \omega}$$

Forward Loop Gain

$$CL(\omega) := \frac{G(\omega)}{1 + \frac{G(\omega)}{N}}$$

Closed Loop Gain

BANDWIDTH AND PHASE MARGIN

$\omega := 10.0kHz$

$\omega c := root(|G(\omega)| - N, \omega)$ $\quad \frac{\omega c}{2 \cdot \pi} = 20\,kHz$

Loop Bandwidth

$$\frac{180}{\pi} \cdot \arg(G(\omega c)) + 180 = 49.443$$

Phase Margin

12. Design of an Active Loop Filter Using the Differential Phase Detector Outputs

Introduction

This chapter investigates the design and performance of a loop filter designed using the differential phase detector outputs, fr and fp. This topology bypasses the charge pump and is most advantageous when used with a PLL with a bad charge pump. Since spurs and phase noise are based on properties of the charge pump, these parameters may be different for this type of filter. For PLLs with a well balanced and low-leakage charge pump, other active loop filter topologies are recommended that use the charge pump output. The reason for using an active filter is typically to get an increased tuning voltage to the VCO. Many modern day PLLs do not have these differential phase detector outputs, which makes this approach impossible.

Loop Filter Topology

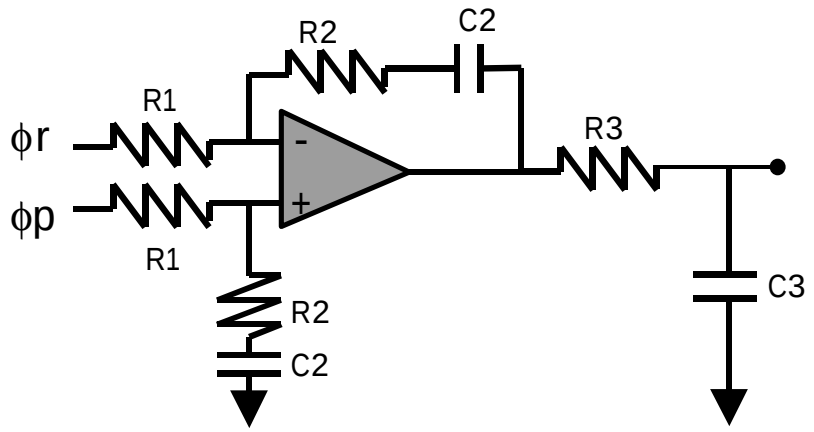


Figure 1 *Active Filter Topology Used*

The transfer function of the filter is given by:

$$Z(s) = \frac{1 + s \bullet T2}{s \bullet T \bullet (1 + s \bullet T1)}$$

where

$$T2 = R2 \bullet C2$$
$$T1 = R3 \bullet C3$$
$$T = R1 \bullet C2$$

The open loop response is given by:

$$G(s)/N = \frac{Kv \bullet Kvco \bullet (1 + s \bullet T2)}{N \bullet T \bullet s^2 \bullet (1 + s \bullet T1)}$$

From the chapter on a second order passive filter, this transfer function has many similarities. If the following substitutions are applied to expression for the open loop response for the second order filter, then the result is the transfer function for this loop filter topology. In these equations, Kv represents the maximum voltage output level of the phase detector outputs.

$$T \Rightarrow Ctot$$
$$Kv \Rightarrow Kf$$

The case where ***R3 = C3 = 0*** presents a special case and has different equations, but is a topology that is sometimes used. This approach will be referred to as the alternative approach, and the case where ***T1>0*** will be referred to as the standard approach. In either case, the equations for the time constants and filter components are shown in Table 1.

Component	Standard Approach	Alternative Approach
T1	$T1 = \frac{\sec(f) - \tan(f)}{wc}$	***0***
T2	$T2 = \frac{1}{wc^2 \bullet T1}$	$wc \bullet \tan f$
T	$T = \frac{Kv \bullet Kvco}{N \bullet wc^2} \bullet \sqrt{\frac{1 + wc^2 \bullet T2^2}{1 + wc^2 \bullet T1^2}}$	$T = \frac{Kv \bullet Kvco}{N \bullet wc^2 \bullet \cos f}$
C2	*Choose this value*	*Choose this value*
R2	$\frac{T2}{C2}$	$\frac{T2}{C2}$
R1	$\frac{T}{C2}$	$\frac{T}{C2}$
C3	*Choose this at least four times the VCO input capacitance. Preferably at least 200 pF.*	***0***
R3	$\frac{T3}{C3}$	***0***

Table 1 *Loop Filter Time Constants and Component Values*

Conclusion

This chapter has presented design equations that can be used with the differential phase detector outputs. This approach is generally not recommended, because it requires an op-amp and most PLLs do not have these differential output pins. The reader should also be very aware of the states of the outputs. For instance, when this type of loop filter is used with National Semiconductor's LMX2301/05/15/20/25 PLLs, it is necessary to invert either fr or fp.

There are other approaches to loop filter design using these differential outputs. One such approach is to omit the components ***R3*** and ***C3***. In this case, ***T1*** becomes zero and ***T2*** becomes ***wc•tan(f).*** This topology is more popular with older PLL designs than newer ones.

The lock time can be predicted with a formula, but the phase noise and spurs for this filter differ than those in a passive filter. The ***BasePulseSpur*** and ***1HzNoiseFloor*** are different, since the charge pump has been bypassed.

References

[1] AN535 *Phase-Locked Loop Design Fundamentals* Motorola Semiconductor Products, 1970

ACTIVE FILTER DESIGN USING THE DIFFERENTIAL PHASE DETECTOR OUTPUTS

USER NEEDS TO ENTER THESE:

$Kvco := 10\frac{MHz}{volt}$ VCO Gain

$Kv := 4 \cdot volt$ Phase Detector Voltage Gain

$Fout := 700MHz$ RF output frequency

$Fcomp := 100kHz$ Comparison Frequency

$Fc := 2 \cdot kHz$ Loop Bandwidth

$\phi := 50deg$ Phase Margin

CALCULATIONS FOR BOTH APPROACHES

$N := \frac{Fout}{Fcomp}$ $N = 7 \cdot 10^{3}$ $\omega c := 2 \cdot \pi \cdot Fc$

STANDARD APPROACH

LOOP FILTER CALCULATION

$$T1 := \frac{\sec(\phi) - \tan(\phi)}{\omega c} \qquad T2 := \frac{1}{\omega c^2 \cdot T1} \qquad T := \frac{Kv \cdot Kvco}{N \cdot \omega c^2} \cdot \sqrt{\frac{1 + \omega c^2 \cdot T2^2}{1 + \omega c^2 \cdot T1^2}}$$

$$C2 := 1 \cdot nF \qquad R2 := \frac{T2}{C2} \qquad R1 := \frac{T}{C2} \qquad C3 := 1000 pF \qquad R3 := \frac{T1}{C3}$$

COMPONENTS

$C2 = 1.000\,nF$ $\qquad$ $R1 = 99.421\,k\Omega$

$C3 = 1.000\,nF$ $\qquad$ $R2 = 218.633\,k\Omega$

$R3 = 28.964\,k\Omega$

LOOP FILTER SIMULATION

$$Z(\omega) := \frac{1 + C2 \cdot R2 \cdot i \cdot \omega}{R1 \cdot i \cdot \omega \cdot C2 \cdot (1 + i \cdot \omega \cdot R3 \cdot C3)}$$ Loop Filter Impedance

$$G(\omega) := \frac{Kv \cdot Kvco \cdot Z(\omega)}{i \cdot \omega}$$ Forward Loop Gain

$$CL(\omega) := \frac{G(\omega)}{1 + \frac{G(\omega)}{N}}$$ Closed Loop Gain

LOOP BANDWIDTH AND PHASE MARGIN

$\omega := 10.0 kHz$

$$\frac{root(|G(\omega)| - N, \omega)}{2 \cdot \pi} = 20.0\,kHz$$ Loop Bandwidth

$$\arg(G(\omega c)) \cdot \frac{180}{\pi} + 180 = 50$$ Phase Margin

ALTERNATIVE APPROACH WITH T1 = 0

LOOP FILTER CALCULATION

$$T2 := \frac{\tan(\phi)}{\omega c} \qquad T := \frac{Kv \cdot Kvco}{N \cdot \omega c^2 \cdot \cos(\phi)}$$

$$C2 := 1 \cdot nF \qquad R2 := \frac{T2}{C2} \qquad R1 := \frac{T}{C2}$$

COMPONENTS

$C2 = 1.000\,nF$ $R1 = 56.298\,k\Omega$

$R2 = 94.837\,k\Omega$

LOOP FILTER SIMULATION

$$Z(\omega) := \frac{1 + C2 \cdot R2 \cdot i \cdot \omega}{R1 \cdot i \cdot \omega \cdot C2}$$ Loop Filter Impedance

$$G(\omega) := \frac{Kv \cdot Kvco \cdot Z(\omega)}{i \cdot \omega}$$ Forward Loop Gain

$$CL(\omega) := \frac{G(\omega)}{1 + \frac{G(\omega)}{N}}$$ Closed Loop Gain

LOOP BANDWIDTH AND PHASE MARGIN

$\omega := 10.0\,kHz$

$\omega c := root(|G(\omega)| - N, \omega)$ $\frac{\omega c}{2 \cdot \pi} = 2.000\,kHz$ Loop Bandwidth

$\arg(G(\omega c)) \cdot \frac{180}{\pi} + 180 = 50$ Phase Margin

13. The Impact of Loop Filter Parameters and Filter Order on Reference Spurs

Introduction

It has been shown that the reference spur levels are directly related to the spur gain, whether they are leakage or pulse dominated. This chapter investigates methods of minimizing the spur gain under various conditions. First, it will be shown why choosing all the pole ratios (T31, T41,…) equal to one always yields the lowest spur gain filter. Then, the impact of other loop filter design parameters on the spur gain will also be investigated. Recall that in a previous chapter, the impact of various parameters was analyzed in the case that the loop filter was not redesigned. In this chapter, it will be assumed that the loop filter is redesigned. For instance, having a bigger VCO gain increases spur levels if the loop filter is not redesigned. But, it turns out that it has no impact if the loop filter is redesigned to have the same loop bandwidth.

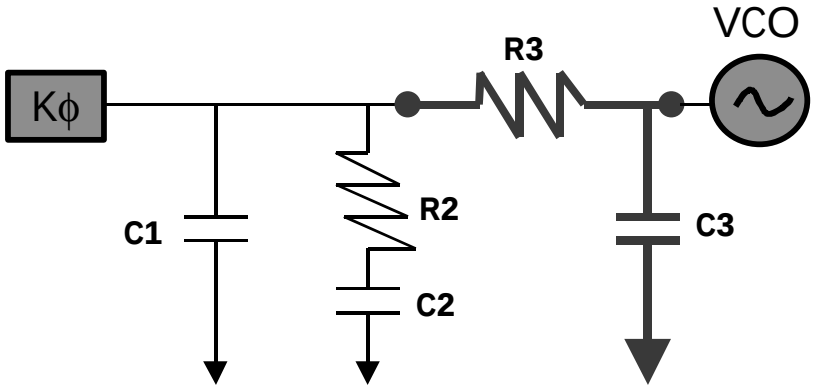


Figure 1 *Basic Passive Loop Filter Topology*

Minimization of Spur Gain

Since the spur levels relate directly to the spur gain of the PLL, the problem is therefore reduced to minimizing the spur gain under the constraints of a constant loop bandwidth and phase margin. The poles of the filter will be represented by ***Ti***, (***i =1,3,4, …k***). Note that ***T2*** is the zero of the filter and therefore the index skips over two. The filter order is ***k***, which is assumed to be greater than two. ***T1(i)*** is intended to mean the ratio of pole ***Ti*** to the pole ***T1***. This number can range from zero to one. Note that ***T1(1)*** = ***1***. The spur gain at any frequency can be expressed as:

$$|G(w)| = \frac{Kf \bullet Kvco}{Ctot \bullet w^2} \bullet \sqrt{\frac{1 + w^2 \bullet T2^2}{\prod_{i=1,3,4,\ldots k} (1 + w^2 \bullet Ti^2)}} \tag{1}$$

However ***Ctot*** is not constant. Recall:

$$Ctot = \frac{Kf \bullet Kvco}{N \bullet wc^2} \bullet \sqrt{\frac{1 + wc^2 \bullet T2^2}{\prod_{i=1,3,4,\ldots k} (1 + wc^2 \bullet Ti^2)}} \tag{2}$$

Substituting this in gives the following expression for ***G(s)***:

$$|G(s)| = N \bullet \frac{wc^2}{w^2} \bullet \sqrt{\frac{1+w^2 \bullet T2^2}{1+wc^2 \bullet T2^2} \bullet \prod_{i=1,3,4,...k} \frac{(1+wc^2 \bullet Ti^2)}{(1+w^2 \bullet Ti^2)}} \tag{3}$$

The above equation eliminates all of the component values from the equations, but still leaves the time constants to be calculated. However, there are three equations that relate the time constants to known design parameters. It therefore follows that the spur gain can be expressed uniquely in terms of design parameters. The equations relating the time constants to filter parameters were given in the section for the standard method for loop filter design and are presented below:

$$T1 = \frac{\sec f - \tan f}{wc \bullet \sum_{i=1,3,4,...k} T1(i)} \tag{4}$$

$$Ti = T1 \bullet T1(i) = \frac{\sec f - \tan f}{wc \bullet \sum_{i=1,3,4,...k} T1(i)} \bullet T1(i) \tag{5}$$

$$T2 = \frac{1}{wc^2 \bullet \sum_{i=1,3,4,...k} Ti} = \frac{1}{wc \bullet (\sec f - \tan f)} \tag{6}$$

Substituting (4) , (5), and (6) into (3) yields the spur gain in terms of design parameters.

$$|G(s)| = \frac{N}{r^2} \bullet \sqrt{\frac{r^2+x^2}{1+x^2} \bullet \prod_{i=1,3,4,...k} \left[\frac{\left(\sum_{j=1,3,4,...k} T1(j) \right)^2 + T1(i)^2 \bullet x^2}{\left(\sum_{j=1,3,4,...k} T1(j) \right)^2 + T1(i)^2 \bullet x^2 \bullet r^2} \right]} \tag{7}$$

The following terms are defined above:

$$x = \sec f - \tan f$$

$$r = \frac{Spur\ Frequency}{Loop\ Bandwidth} = \frac{Fspur}{Fc} \tag{8}$$

Since there is a leading $\frac{1}{r^2}$ term, it should be clear that the spur gain is minimized for the smallest values of ***r***, which corresponds to minimizing the loop bandwidth. Some other things that are a little less obvious are the relationship of spur gain to the parameter ***x*** and the relationship of spur gain to the poles ratios of the filter. Since ***r*** can be assumed to be greater than one, it can be shown that (7) is a decreasing function in ***T1(i)*** for ***i=1,3,...k***. However, these pole ratios can not exceed one, since ***T1*** is by definition the largest pole. From this observation comes the fundamental result that for minimum spur levels, the pole ratios should all be chosen to be one. However, choosing all of the pole ratios to be one can yield a loop filter with a very small capacitor next to the VCO, which can be impacted by the VCO input capacitance. In the case of using the improved design equations for a fourth order filter, this capacitor would be zero. So there is often a good reason why the pole ratios should be chosen less than one.

One can reason from equation (7) that this function is a decreasing function of $|x|$, because if $r > 1$, this makes each one of the fractional parts decreasing functions in $|x|$, therefore the whole function is decreasing in $|x|$. So, for the minimum spur levels, this is equivalent to minimizing equation (8). Going through this exercise shows that this function is an increasing function in f in the interval from 0 to 90 degrees, and therefore minimizing the spur gain corresponds to minimizing the phase margin. However, in practice, the impact of changing the phase margin typically does not have much of an impact on spurs. In the chapter on lock time, the second order function implies that lower phase margins also yield faster lock times. However, computer simulations using the 4th order model show that the phase margin that yields the fastest lock time is usually about 48 degrees. Therefore, it makes sense to design for a phase margin near 48 degrees, because this gives more freedom to adjust the loop bandwidth, which has a far greater impact on spur levels than phase margin.

Relationship to Parameter	Leakage Dominated Spurs	Mismatch Dominated Spurs
Charge Pump Leakage, i_{leak}	$20\bullet\log(i_{leak})$	N/A
Mismatch, M	N/A	Correlated to $\lvert M - \delta \rvert$
N Value, N	$20\bullet\log(N)$	$20\bullet\log(N)$
Phase Margin	Weak Inverse Correlation, see Table 2	
VCO Gain, Kvco	Independent	Independent
loop Bandwidth, wc	$40\bullet\log(\omega c)$	$40\bullet\log(\omega c)$
Ratio of T3 to T1	See Table 2, depends on phase margin	
Comparison Frequency	$-40\bullet\log(Fcomp)$	$-40\bullet\log(Fcomp)$
r = Fcomp/wp	$-40\bullet\log(r)$	$-40\bullet\log(r)$
Charge Pump Gain, Kf	$-10\bullet\log(K\phi)$	Independent

Table 1 *Reference Spur Gain vs. Various Loop Filter Parameters*

From Table 1, it follows that the loop bandwidth, comparison frequency, and ***N*** value have the largest influence on the spur level. If one considers the ratio of the comparison frequency to the loop bandwidth, then this is a rough indicator. The ***N*** value is also relevant, but is related to the comparison frequency. Larger charge pump gains yield lower leakage dominated spurs, because they yield larger capacitor values in the loop filter. The reader should be very careful to realize that these values assume that the loop filter is redesigned and optimized. If the loop filter is not redesigned, then the results will be very different. These results were derived in a previous chapter.

Formula (7) shows that the spur gain of a third order filter is given by:

$$SG = 20\bullet\log(N) - 40\bullet\log(r) + 10\bullet\log\left|\frac{r^2+x^2}{1+x^2}\bullet\frac{(1+T31)^2+T31^2\bullet x^2}{(1+T31)^2+T31^2\bullet x^2\bullet r^2}\bullet\frac{(1+T31)^2+x^2}{(1+T31)^2+x^2\bullet r^2}\right|$$

So the ***20•log(N)*** term shows the clear dependence on ***N***, and therefore, Table 2 assumes an ***N*** value of one, to which this ***20•log(N)*** must be added. Note that these equations assume that the filter is redesigned. If this is not the case, then it turns out that the spurs are not impacted much by the ***N*** value. The phase margin and ***r*** values are given. From this, go and find the main block, and then find the corresponding value of the ***N=1*** normalized spur gain. To this, add ***20•log(N)*** to get the total spur gain.

		r										
		3	5	10	15	20	25	50	100	200	500	1000
T31 = 0	f=30	-15.4	-23.6	-35.3	-42.3	-47.3	-51.2	-63.2	-75.2	-87.3	-103.2	-115.2
	f=40	-14.1	-22.0	-33.6	-40.5	-45.5	-49.3	-61.3	-73.4	-85.4	-101.3	-113.4
	f=50	-12.9	-20.3	-31.5	-38.4	-43.3	-47.2	-59.2	-71.2	-83.3	-99.2	-111.2
	f=60	-11.7	-18.4	-29.1	-35.9	-40.8	-44.6	-56.5	-68.6	-80.6	-96.5	-108.6
	f=70	-10.6	-16.5	-26.1	-32.5	-37.3	-41.1	-52.9	-64.9	-77.0	-92.9	-104.9
T31 = .25	f=30	-14.9	-23.5	-37.5	-46.8	-53.7	-59.3	-77.0	-94.9	-113.0	-136.8	-154.9
	f=40	-13.5	-21.6	-34.7	-43.6	-50.3	-55.7	-73.2	-91.1	-109.2	-133.0	-151.1
	f=50	-12.3	-19.6	-31.8	-40.1	-46.6	-51.8	-69.0	-86.8	-104.8	-128.6	-146.7
	f=60	-11.2	-17.7	-28.7	-36.3	-42.3	-47.2	-63.8	-81.5	-99.4	-123.2	-141.3
	f=70	-10.3	-15.9	-25.3	-32.0	-37.3	-41.8	-57.2	-74.3	-92.1	-115.9	-134.0
T31 = .50	f=30	-14.8	-24.0	-39.2	-49.1	-56.3	-62.0	-79.9	-97.9	-116.0	-139.8	-157.9
	f=40	-13.4	-21.7	-36.0	-45.5	-52.6	-58.3	-76.1	-94.1	-112.1	-136.0	-154.0
	f=50	-12.1	-19.5	-32.5	-41.6	-48.5	-54.0	-71.7	-89.6	-107.7	-131.5	-149.6
	f=60	-11.0	-17.4	-28.9	-37.2	-43.8	-49.1	-66.4	-84.3	-102.3	-126.1	-144.2
	f=70	-10.2	-15.7	-25.1	-32.2	-38.0	-42.9	-59.4	-77.0	-94.9	-118.8	-136.8
T31 = .75	f=30	-14.8	-24.2	-39.8	-49.8	-57.1	-62.8	-80.8	-98.8	-116.8	-140.7	-158.8
	f=40	-13.3	-21.8	-36.4	-46.2	-53.4	-59.1	-76.9	-94.9	-113.0	-136.9	-154.9
	f=50	-12.0	-19.5	-32.9	-42.2	-49.2	-54.8	-72.5	-90.5	-108.5	-132.4	-150.5
	f=60	-11.0	-17.4	-29.0	-37.6	-44.3	-49.7	-67.2	-85.1	-103.1	-127.0	-145.0
	f=70	-10.2	-15.6	-25.1	-32.3	-38.3	-43.3	-60.1	-77.8	-95.8	-119.6	-137.7
T31 = 1.0	f=30	-14.8	-24.3	-39.9	-50.0	-57.3	-63.0	-80.9	-99.0	-117.0	-140.9	-159.0
	f=40	-13.3	-21.8	-36.6	-46.3	-53.6	-59.2	-77.1	-95.1	-113.2	-137.0	-155.1
	f=50	-12.0	-19.5	-32.9	-42.3	-49.4	-54.9	-72.7	-90.7	-108.7	-132.6	-150.7
	f=60	-11.0	-17.3	-29.1	-37.7	-44.4	-49.8	-67.4	-85.3	-103.3	-127.2	-145.2
	f=70	-10.2	-15.6	-25.1	-32.4	-38.4	-43.4	-60.3	-78.0	-96.0	-119.8	-137.9

Table 2 *Relative N=1 Normalized Spur Gains for a Third Order Filter*

The table above is a powerful design tool to figure out how to adjust the phase margin, T31 value, and/or loop bandwidth to get just the right level of spurious attenuation, so that the lock time of the PLL can be minimized.

Choosing the Right Filter Order

If one assumes 50 degrees phase margin and takes formula (7) and assumes that all the poles are equal, then the relative attenuation of a filter over a second order filter can be calculated. Some areas are darkly shaded to indicate that the loop filter order is too high and not practical.

		Ratio of Comparison Frequency To Loop Bandwidth						
		1000	100	50	20	10	5	3
Loop Filter Order	3	40.63	20.64	14.68	7.08	2.20	-0.58	-0.9
	4	76.51	36.57	27.72	10.09	1.75	-1.71	-1.5
	5	109.37	49.53	31.94	11.01	0.57	-2.60	-1.95
	6	140.02	60.33	37.16	10.79	-0.70	-3.25	-2.4

Table 3 *Spur Improvement for Various Order Filters Above a Second Order Filter*

Although the table does contain some approximations, it does establish an upper estimate for the attenuation that can be achieved. Notice that when the comparison frequency is large relative to the loop bandwidth, there is much more advantage in building higher order filters. Of course in these cases, spurs are often not as much of an issue. The chart also implies that a third order loop filter (two poles) only makes sense if the comparison frequency is at least ten times the loop bandwidth. Although the maximum attenuation is for the case when $T1 = T3 = ... = Tk$, it sometimes makes sense to design for $T1 > T3 > ... > Tk$, in order to keep the capacitors large enough as to not be distorted by the VCO input capacitance and to better justify the approximations made.

Conclusion

This chapter investigated the impact of designing loop filters of higher than second order and when it makes sense to do so. One fundamental result is that the lowest reference spurs occur when the pole ratios are chosen equal to one. However, choosing all pole ratios equal to one can yield very small capacitor values next the VCO, which are easily be impacted by the VCO input capacitance. If one is designing a fourth order filter using the improved calculations, this would imply that $C4 = 0$. When confronted with a situation where the spur to be filtered is less than $1/10^{th}$ of the loop bandwidth, the fastlock feature is often a better approach to spur reduction than higher order filters.

14. Using the Fastlock Feature for PLL Design

Introduction

In PLL design, there is a classical trade-off between faster switching time and lower reference spurs. If one increases the loop bandwidth, then the lock time decreases at the expense of increasing the spur levels. If one decreases the loop bandwidth, the spurs decrease at the expense of increasing the lock time. The concept of fastlock is to use a wide loop bandwidth when switching frequencies, and then switch a narrow loop bandwidth when not switching frequencies. Fastlock can also be used in situations where lock time and RMS phase error are traded off, or in situations where lock time and phase noise outside the loop bandwidth are traded off.

Fastlock Description

Fastlock is a feature of some PLLs that allows a wide loop bandwidth to be used for locking frequencies, and a narrower one to be used in the steady state. This can be used to reduce the spur levels, or phase noise outside the loop bandwidth. Fastlock is typically intended for a second order filter. It can be used in higher order loop filter designs, but the pole ratios (***T31***, ***T41***, and so on) need to be small, otherwise, when the wider loop bandwidth is switched in, the filter becomes very unoptimized and the lock time increases. For this reason, this chapter focuses only on the use of fastlock for a second order design.

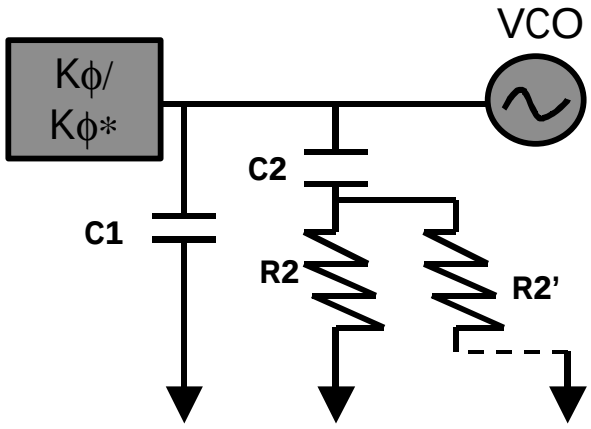


Figure 1 *Second Order Filter Using Fastlock*

When the PLL is in the locked state, charge pump gain Kf is used and resistor ***R2'*** is not grounded, therefore having no impact. When the PLL switches frequency, the charge pump gain is increased by a factor of M^2 to Kf^* . Resistor ***R2'*** is also switched in parallel with ***R2***, making the total resistance ***R2**** = ***R2*** || ***R2'*** = ***R2/M***. Recall that the loop filter impedance for the second order filter is given by:

$$Z(s) = \frac{1 + s \bullet C2 \bullet R2}{s \bullet (C1 + C2) \bullet \left(1 + s \bullet \frac{C1 \bullet C2 \bullet R2}{C1 + C2}\right)} = \frac{1 + s \bullet T2}{s \bullet Ctot \bullet (1 + s \bullet T1)}$$

$$T2 = R2 \bullet C2$$

$$T1 = \frac{R2 \bullet C2 \bullet C1}{Ctot}$$

$$Ctot = C1 + C2$$

	Normal Mode	Fastlock Mode
M	$\sqrt{\frac{Kf^*}{Kf}}$	$\sqrt{\frac{Kf^*}{Kf}}$
R2'	$\frac{R2}{M-1}$	$\frac{R2}{M-1}$
Equivalent Resistance, R2*	R2	$\frac{R2}{M}$
Charge Pump Gain	Kϕ	Kϕ*
Zero T2	T2	$\frac{T2}{M}$
Pole T1	T1	$\frac{T1}{M}$
Loop Bandwidth	ωc	M●ωc
Theoretical Lock Time	LT	$\frac{LT}{M}$

Table 1 *Comparison of Filter Parameters between Normal Mode and Fastlock Mode*

From Table 1, one could conclude that if the charge pump was normally 1 mA, and then was switched to 4 mA, ***M*** would be two and there would be a theoretical 50% improvement in lock time. Another way of thinking about this is that the loop bandwidth could be decreased to half of its original value, thus making a theoretical 12 dB improvement in reference spurs. However, this disregards the fact that there is a glitch when fastlock is disengaged, and this glitch can be very significant.

The Fastlock Disengagement Glitch

Cause and Behavior of the Glitch

When the fastlock is disengaged, a frequency glitch is created. This glitch can be caused by parasitic capacitances in the switch that switches out the resistor ***R2'***, and also imperfections in charge pump. When the switch is disengaged, a small current is injected into the loop filter. It therefore follows that the size of the glitch is loop filter and PLL specific. One possible way to simulate the glitch is to model the unwanted charge injected into the loop filter as a delta function times a proportionality constant. From this, one can see why the glitch size is greater for an unoptimized filter and inversely proportional to charge pump gain, assuming an optimized loop filter of fixed loop bandwidth. Experimental results show that the ratio, M, does not have much impact on this glitch, only the charge pump gain used in the steady state. For instance, if the charge pump gain was 100 uA in normal mode and 800 uA in fastlock mode, then the glitch caused by disengaging fastlock would be the same if the current was increased from 100 uA to 1600 uA in fastlock mode.

The glitch also decreases as the loop bandwidth decreases. This can yield some unanticipated results. For instance, one would think that a loop filter with 2 KHz loop bandwidth using fastlock would take twice the time to lock as one with a 4 KHz loop bandwidth using fastlock. However, it could lock faster than this since the fastlock glitch for the 2 KHz loop filter is less. In other words, the 4 KHz loop bandwidth filter would lock faster than the 2 KHz loop filter, but maybe not twice as fast. Increasing the capacitor ***C1*** or the pole ratios decrease the glitch, while increasing ***C2*** makes the glitch slightly larger.

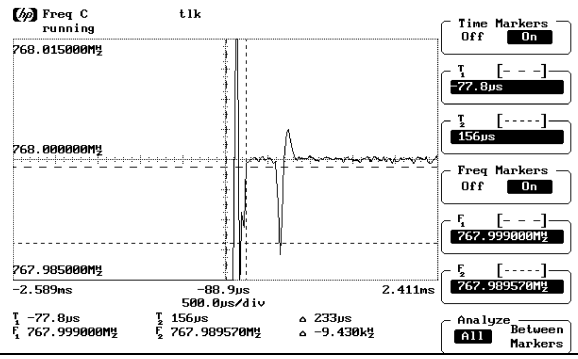
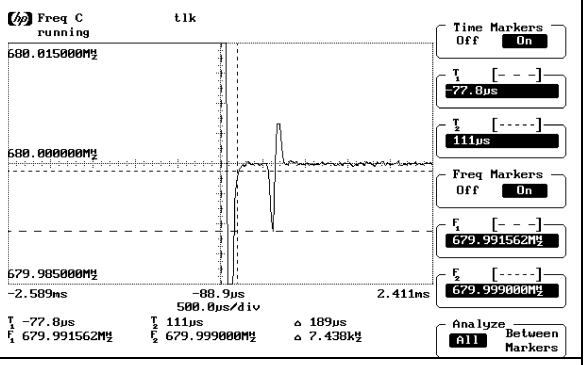
Switching from 680 – 768 MHz	Switching from 768 – 680 MHz
	
This shows a lock time of 233 uS and a fastlock glitch of 10.4 KHz	*This shows a lock time of 189 uS and a fastlock glitch of 8.4 KHz*

Figure 1 *Fastlock Disengagement Glitch*

Optimal Timing for Fastlock Disengagement

For optimal lock time, the fastlock should be disengaged at a time such that the magnitude of this glitch is about the magnitude of the ringing of the PLL transient response. If fastlock is disengaged too early, then the full benefits of the fastlock are not realized. If it is disengaged too late, then the settle time for the glitch becomes too large of a proportion of the lock time. Figure 2 shows the lock time when the fastlock glitch is taken into consideration.

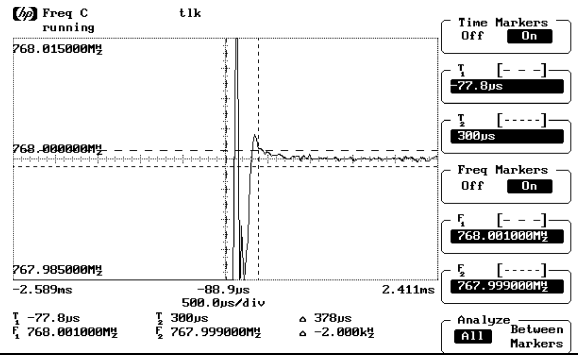
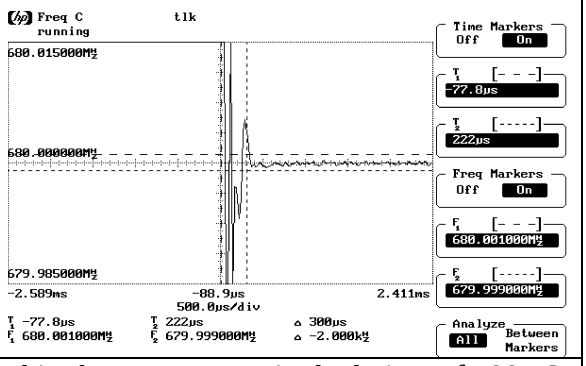
Switching from 680 – 768 MHz	Switching from 768 – 680 MHz
	
This shows a composite lock time of 378 uS with a fastlock timeout of 100 uS	*This shows a composite lock time of 300 uS with a fastlock timeout of 100 uS*

Figure 2 *Lock Time Using Optimal Fastlock Timeout of 100 uS*

Disadvantages of Using Fastlock

Increased In-Band Phase Noise

Since fastlock requires that a higher current is switched in during frequency acquisition, this requires that the PLL is run in less than the highest current mode. Recall from the phase noise chapter that the in-band phase noise is typically better for the higher charge pump gain.

Higher Order Loop Filters

Another disadvantage of using fastlock is that if one builds a third or higher order filter with much considerable spur attenuation, then it is likely not to work well with fastlock. Fastlock is most effective for second order loop filters, or higher order filters with small pole ratios.

Benefits of Using Fastlock

$M = \sqrt{\frac{Kf^*}{Kf}}$	Loop Bandwidth Increase	Theoretical Lock Time Reduction	R2'
2:1	2 X	50 %	R2
3:1	3 X	67 %	$\frac{R2}{2}$
4:1	4 X	75 %	$\frac{R2}{3}$
M:1	M X	$100 \bullet \left(1 - \frac{1}{M}\right)$ %	$\frac{R2}{M-1}$

Table 2 *Theoretical Benefits of Using Fastlock*

The theoretical benefits of using fastlock presented in Table 2 should be interpreted as an upper bound for expected improvement, since it disregards the glitch caused when disengaging fastlock. Typically, in the type of fastlock when the charge pump current is increased from 1X to 4 X (***M=2***), the actual benefit of using fastlock is typically about 30%. In the type of fastlock where the charge pump current is increased from 1X to 16X (***M=4***), the actual benefit of using fastlock is typically closer to a 50% improvement. These typical numbers are based on National Semiconductor's LMX233X and LMX235X PLL families.

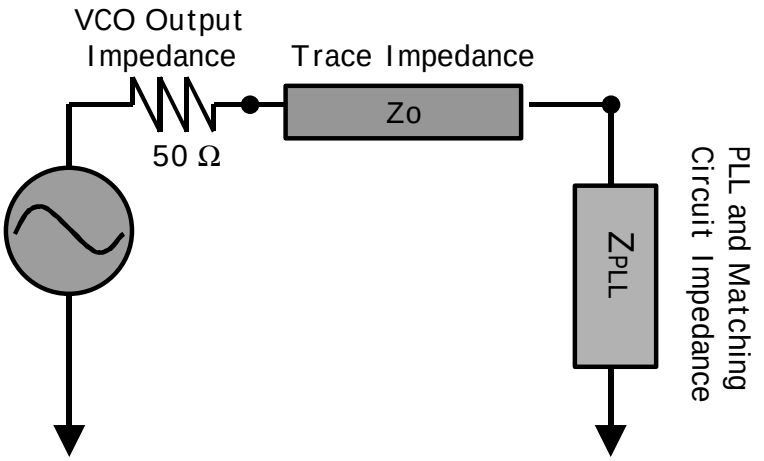
Conclusion

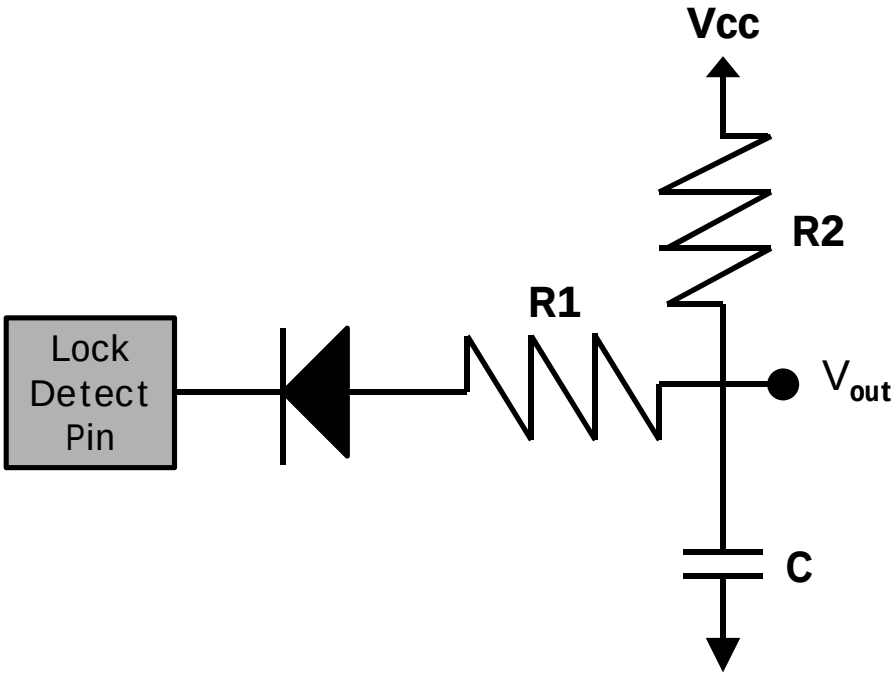
Fastlock is most beneficial in applications where the frequency offset of the most troublesome spur is less than ten times the loop bandwidth. In these situations, higher order filters have little real impact on the spur. As the spur offset frequency becomes farter from the carrier, higher order filters become more practical. An important issue with fastlock is the glitch created by when it is disengaged. This is application specific, but it can take a significant portion of the lock time.

References

[1] Davis, Craig, et.al. *A Fast Locking Scheme for PLL Frequency Synthesizers. National Semiconductor AN-1000*

Additional Topics





15. Lock Detect Circuit Construction and Analysis

Introduction

Although many newer PLLs have a lock detect pin that give a logic level output to indicate whether or not the PLL is in lock, there are still many PLLs, including the LMX233X series from National Semiconductor, that do not put out a logic level signal to indicate whether or not the part is in lock; external circuitry is necessary in order to make meaningful sense of the signal. This chapter discusses the design and simulation of such a circuit.

Using the Analog Lock Detect Pin

The state of analog lock detect pin is high when the charge pump is off and low when the charge pump turns on. When viewed with an oscilloscope, one can observe narrow negative pulses that occur when the charge pump turns on. When the PLL is in the locked state, these pulses are on the order of 25-70 nS in width; however, this number can vary based on the VCO gain, loop filter transfer equations, phase detector gain, and other factors, although it should be constant for a given application. For some PLLs, the output is open drain and requires a pull-up resistor to see the pulses.

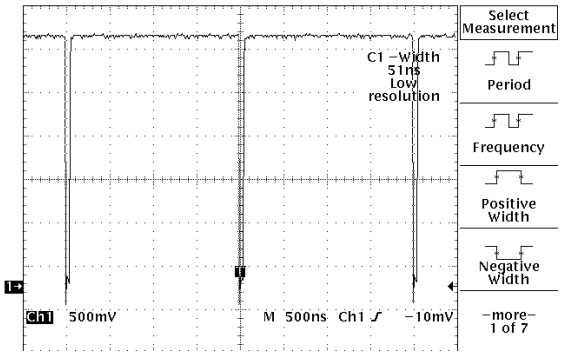


Figure 1 *Lock Detect Pin Output for a PLL in the Locked State*

When the PLL is not in the locked state, the average width of these pulses changes. The information concerning the PLL in or out of the locked state is in no individual pulse, but rather in the average pulse width. If the VCO kept on but disconnected from the charge pump, then the signal from the lock detect pin will have a duty cycle that oscillates between a low and high duty cycle. However, this is unrealistic, since the PLL tries to keep the VCO in phase. When the VCO is connected to the PLL, but is off frequency, the pulse width is much more predictable and closer to being constant. The pulses are sort of triangular due to the turn on times of transistors and other effects. However, they will be treated as rectangular for the purpose of simplifying the calculations in this chapter. For a ballpark estimate of how much the average width of the pulses will change and a rough idea on how sensitive the circuit is, the average change in the width of the pulses at any given time could be approximated by the difference in the periods of the N counter and the R counter. This result was discussed in a previous chapter concerning the performance of the phase detector. In other words,

$$\textit{Change in Average Pulse Width} = Tlow - Tloc = \frac{1}{Fcomp} - \frac{N}{Fout}$$

Lock Detect Circuit Construction

The basic strategy for the type of lock detect circuit described in this chapter is to integrate over some number of reference periods in order to accumulate some DC value which can then be compared to a threshold value. This comparison can be made with a comparator or transistor. In cases where only a gross lock detect is needed, the lock detect circuit output can be sent directly to the input logic gate, provided the difference in the voltage level produced between the in lock and out of lock conditions is large enough to be recognized as a high or low. Some microprocessors also have A/D input pins that can also be used for this function.

Since the average DC contributions of the pulses are so small relative to the rest of the time, it may be necessary to use unbalanced time constants to maximize sensitivity. The recommended circuit is shown in Figure 1. Note that there are some PLLs in which the lock detect output is open drain, which eliminates the need for the diode. There are still other PLLs with digital lock detect, that eliminate the need for a lock detect circuit entirely.

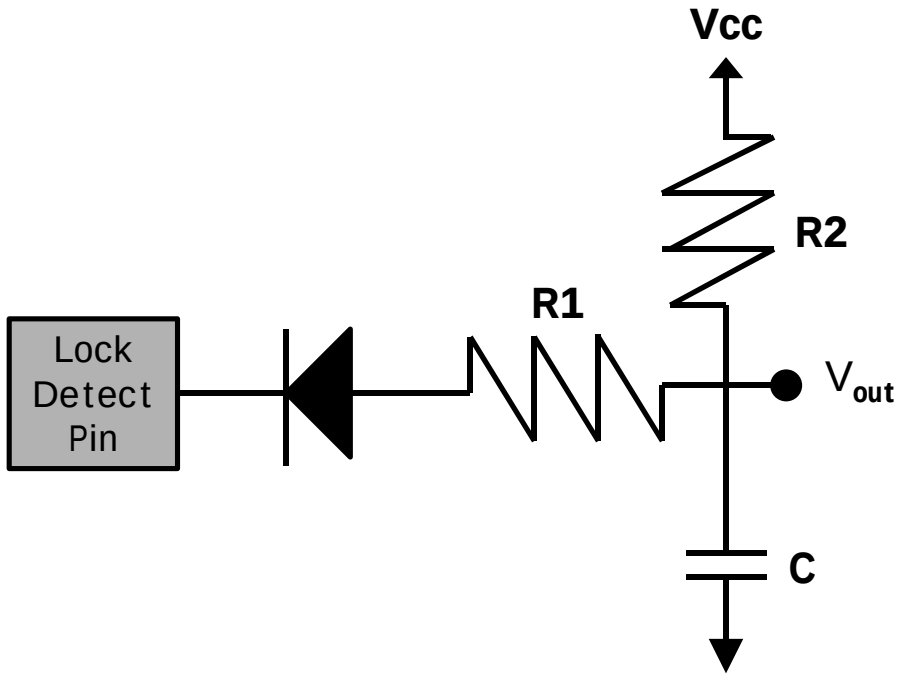


Figure 2 *Lock Detect Circuit*

Theoretical Operation of the Lock Detect Circuit

Consider the event when the lock detect pin first goes to its low voltage, V_{OL}. The voltage drop across the diode is V_D. The diode will conduct, and if $R2 >> R1$ then the following holds:

$$V_{out} = -R1 \bullet C \bullet \frac{dV_{out}}{dt} + V_L$$

$$V_L = V_D + V_{OL}$$

What is really of interest is how much does the voltage V_{out} change during the period that the lock detect pin is low. To simplify the mathematics, it is easiest to discretize the problem. The

size of the discrete time step is T_L, which is the time which the lock detect pin stays low. The following definitions can be used to convert the differential equation into a difference equation:

$$V_n = V_{out}(0)$$
$$V_{n+1} = V_{out}(T_L)$$

The above differential equation has the following solution:

$$V_{n+1} = V_L + (V_n - V_L) \bullet b$$
$$b = e^{\frac{-T_L}{R1 \bullet C}}$$

When the lock detect output goes high, then the diode will not conduct, and the capacitor will charge through the resistor $R2$. In an analogous way that was done for the case of the lock detect pin state being low, the results can also be derived for the case when the lock detect pin is high. In this case, T_H represents the time period that the lock detect pin stays high.

$$V_{n+1} = Vcc + (V_n - Vcc) \bullet a$$
$$a = e^{\frac{-T_H}{R2 \bullet C}}$$

Now if one considers the two cases for V_n, then a general expression can be written for V_n. For sufficiently large n, the series will alternate between two steady state values. Call these two values V_{High} and V_{Low}. These values can be solved for by realizing that the initial voltage when the lock detect pin just goes low will be V_{High} and the final voltage will be V_{Low}. Also, the initial voltage when the lock detect pin just goes high will be V_{Low} and the final voltage will be V_{High}. This creates the following system of two equations and two unknowns.

$$V_{Low} = V_L + (V_{High} - V_L) \bullet b$$

$$V_{High} = Vcc + (V_{Low} - Vcc) \bullet a$$

This system of equations has the following solution:

$$V_{Low} = Vcc + \frac{(1-b) \bullet (V_L - Vcc)}{1 - a \bullet b}$$
$$V_{High} = V_L + \frac{(1-a) \bullet (Vcc - V_L)}{1 - a \bullet b}$$

Lock Detect Circuit Design

The above expressions for V_{Low} and V_{High} show what two values the voltage will oscillate between in the locked condition, once the component values are known. These equations can be worked backwards to solve for component values as well. For design of the circuit, the following information is needed.

T_{lock} The width of the pulses in the locked condition. This should be around 25 nS for the 4X current mode and 50 nS for the 1X current mode.

T_{switch} The width of the LD pulses that are to be detected.

V_{high} The "trip point". In the unlocked condition, the maximum voltage output would be V_{high}. In the locked condition, the voltage output should be higher

Ripple $V_{high} - V_{low}$. This should be a couple hundred millivolts. Designing for too much ripple can cause a noisy circuit, while designing for too little will cause the circuit to take longer to settle to its final values of V_{low} and V_{high}

Using the expressions for V_{high} and V_{low}, the following equations can be derived.

$$a^2 \bullet A + a \bullet B + C = 0$$

$$A = K \bullet \left(V_L - V_{High}\right)$$
$$B = Vcc - V_{High} - K \bullet V_L + K \bullet V_{High}$$
$$C = V_{High} - Vcc$$
$$K = \frac{Vcc - V_{Low}}{V_{High} - V_{Low}}$$

a and b can be solved for as follows:

$$a = \frac{-B + \sqrt{B^2 - 4 \bullet A \bullet C}}{2 \bullet A}$$
$$b = 1 + (a - 1) \bullet K$$

Finally, the components can be solved for. To do so, the capacitor, C, can be chosen arbitrarily. Once C is known, the other components can also be found.

$$R1 = \frac{-T_L}{C \bullet \ln b}$$
$$R2 = R1 \bullet \frac{\ln a}{\ln b} \bullet \frac{T_H}{T_L}$$

Voltages	*Volts*	Times	*ns*	Design Specification	*Volts*
V_D	0.7	T_L	55	$V_{High\ (unlocked)}$	2.1
V_{OL}	0.5	T_H	1600	***Ripple Voltage***	0.1
Vcc	4.1				
Constants		**Components**		**Calculated Values**	
K	2.3333	***Choose C1***	220 pF	***R1***	2.12 *KW*
A	-2.1			***R2***	149.1 *KW*
C	-2			$V_{Low\ (unlocked)}$	2 Volts
a	0.9524				
b	0.8889				

Table 1 *Typical Lock Detect Circuit Design*

Simulation

Note that after the design is done, it is necessary to assure that the lowest voltage in the locked state $V_{Low\ (locked)}$ is higher than the highest voltage unlocked condition $V_{High\ (unlocked)}$. In Table 2, the circuit designed in Table 1 is simulated. The simulation shows that in ten reference cycles, the circuit gets reasonably close to its final steady state values. When the PLL is in lock, the lock detect circuit output voltage will not go below 2.54 Volts; in the unlocked state, the output voltage will not go above 2.10 Volts. This may not seem like much voltage difference, but this is because this circuit is extremely sensitive. If one was to use a pulse width of 100 ns out of lock, then this voltage difference would be much greater.

Table 2 shows the simulation of a lock detect circuit. It is necessary to include a lot of margin for error, since it is very difficult to get an accurate idea of the width of the negative pulses from the lock detect pin. It was also assumed that these pulses were square and of constant period, which may be a rough assumption. Furthermore, as shown below, it does take time for the system to settle down to its final state.

Par.	*Volts*	Components			Times	*nS*	Const.	*Volts*	Locked Parameters		
V_D	0.7	***C***	220	*pF*	T_L	55	α	0.9524	T_{lock}	25	*ns*
V_{OL}	0.5	***R1***	2.1	*KW*	T_H	1600	β	0.8888	b_{lock}	0.9478	*V*
Vcc	2.1	***R2***	149	*KW*							
Vstart	4.5										

Iter.	Vhigh	Vlow		Iter.	Vhigh	Vlow		Steady State Parameters		
0	2.5000	2.3554	*Volts*	***8***	2.2051	2.0933	*Volts*	$V_{High\ (unlocked)}$	***2.0996***	*Volts*
1	2.4385	2.3007	*Volts*	***9***	2.1889	2.0789	*Volts*	$V_{Low\ (}$unlocked)	1.9995	*Volts*
2	2.3864	2.2545	*Volts*	***10***	2.1751	2.0667	*Volts*	***Ripple***	0.1001	*Volts*
3	2.3424	2.2153	*Volts*	***11***	2.1635	2.0564	*Volts*	$V_{Low\ (locked)}$	***2.5451***	*Volts*
4	2.3051	2.1822	*Volts*	***12***	2.1537	2.0476	*Volts*			
5	2.2735	2.1541	*Volts*	***13***	2.1454	2.0402	*Volts*			
6	2.2468	2.1304	*Volts*	***14***	2.1384	2.0340	*Volts*			
7	2.2242	2.1103	*Volts*	***15***	2.1324	2.0287	*Volts*			

Table 2 *Typical Lock Detect Circuit Simulation*

Conclusion

This chapter investigated some of the concepts behind a lock detect circuit design. It is necessary for the designer to have some idea how much the width of the lock detect pulses are changing between the locked and unlocked condition. For both of these situations, T_L was used to represent the width of these lock detect pulses. It is here that it may be necessary to make some gross estimates. Once T_L is known, then the voltage levels of the circuit in the locked and unlocked condition can be calculated. Since there is ripple on this voltage, the minimum voltage level in the locked state should be greater than the maximum voltage level in the high state. From this pulse width, the components can be calculated. Note that there is a trade-off between the sensitivity of the circuit and the time it takes the circuit to respond, as seen in the simulation. Although ripple is undesirable, some ripple must be tolerated in order for the circuit to have sufficient sensitivity. One possible variation of the circuit is to design for a high amount of ripple and then add additional low pass filtering stages afterwards. There is also a specific choice of time constants for theoretical optimum sensitivity. However, assumptions need to be made about the pulse width and the pulse shape, there will be some tinkering left to the lock detect circuit designer.

16. Impedance Matching Issues and Techniques for PLLs

Introduction

This chapter is devoted to matching the VCO output to the PLL input. In most cases, the VCO has a 50 Ω output impedance. However, the PLL input impedance is usually not purely real and not 50 Ω. This can be the cause of many strange problems and a source of tremendous confusion. If the PLL impedance differs greatly from the trace impedance, then power will be reflected back towards the VCO, and significant power will be lost. Furthermore, if the PLL input impedance is not 50 Ω, then this can also cause misinterpretations of the VCO output power level, since it is typically specified for a 50 Ω load. This chapter discusses some of the issues and problems that can arise because of the PLL input impedance not being 50 Ω, and also gives some general matching techniques.

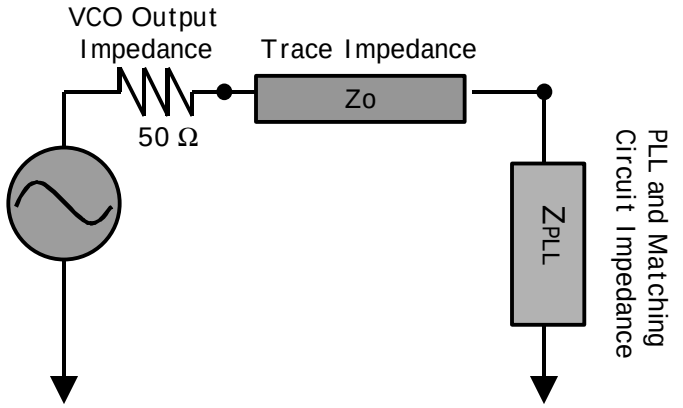


Figure 1 *Circuit Between VCO and PLL*

Calculation of the Trace Impedance

The characteristic impedance of the trace between the PLL and the VCO is determined by the width of the trace, ***W***, the height of the trace above the ground plane, ***H***, and the relative dielectric constant, $\boldsymbol{e_r}$, of the material used for the PCB board. The reader should be careful to not confuse the characteristic impedance of a microstrip line with the input impedance of the PLL or the output impedance of the VCO; these things are all different.

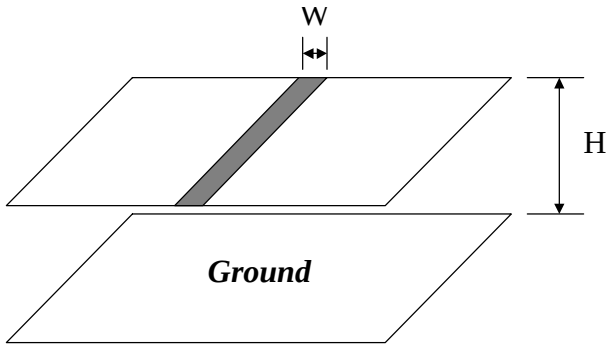


Figure 2 *Calculation of Trace Impedance*

The precise calculation of the trace impedance is rather involved, as is the solution. It is a reasonable approximation to say that the trace impedance is independent of frequency, and it can be approximately calculated with the following formula from reference [1]:

$$Zo \equiv \sqrt{\frac{L}{C}} = \frac{87}{\sqrt{e_r + 1.41}} \bullet ln\left(7.5 \bullet \frac{H}{W}\right)$$

In this formula, L represents the inductance per unit length and C represents the capacitance per unit length. This formula can also be rearranged in order to determine what ratio of height to width is necessary to produce the desired impedance:

$$\frac{H}{W} = \frac{e^{\frac{Zo \bullet \sqrt{e_r + 1.41}}{87}}}{7.5}$$

FR4 is a commonly used material to make PCB boards which has the property that $e_r = 4$. This implies that the ratio of the height to the width is about 0.5 for a 50 Ω trace. In other words, if the thickness from the top layer to the ground plane is 31 mils (thousandths of an inch), then the width of the trace should be 62 mils. There are many online calculators for microstrip impedance, such as reference [1].

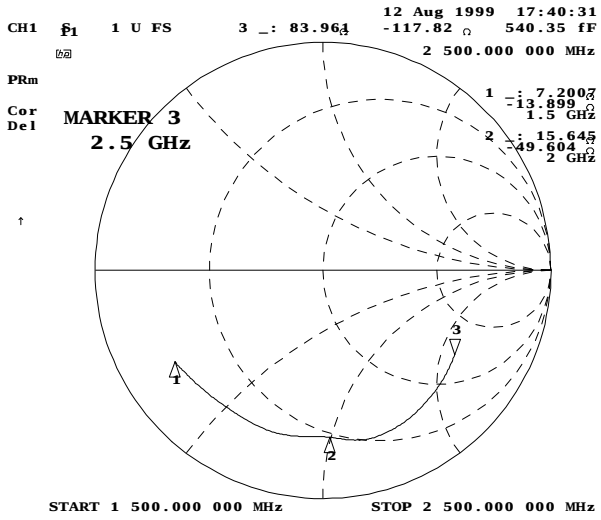


Figure 3 *Smith Chart for Typical Input Impedance for a PLL*

Problems with Having the Load Unmatched to the PCB Trace

Throughout this chapter, the trace impedance will be assumed to be 50 Ω, but the PLL impedance will be assumed to be something different. Note from Smith Chart in Figure 3 that the input impedance of the PLL is far from 50 Ω and is also frequency dependent. It is very common for PLLs to have an input impedance with a negative imaginary part (i.e. Capacitive). In cases where the signal frequency is low, few problems arise. However, for signals in the GHz range, impedance matching problems are common. In the GHz range, a trace of more than a couple centimeters can cause problems if the PLL impedance is poorly matched to the trace

impedance. This typically causes a loss of power and can agitate sensitivity problems in the PLL. Also, since VCOs also put out harmonics, it could cause the prescaler to miscount on a higher harmonic of the VCO if the mismatch is severe enough. In most cases, it is not necessary to use any matching network at all. One way to determine how well the PLL is matched to a 50 Ω line is to calculate the reflection coefficient.

$$r = \sqrt{\frac{(Ra - Ro)^2 + Xa^2}{(Ra + Ro)^2 + Xa^2}} = \sqrt{\frac{\textit{reflected power}}{\textit{transferred power}}}$$

The above formula assumes the impedance of the transmission line is ***Ro***, and the impedance of the PLL is ***Ra*** + ***j•Xa***. If the reflection coefficient is one, then no power is transferred to the PLL, if it is zero, all the power is transferred to the PLL. If the reflection coefficient gets too large, then this could cause problems. These problems are most pronounced when there is a long trace between the VCO and the PLL.

Impedance Matching Strategies

Eliminating the Imaginary Part of the Impedance

Without loss of generality, both the output impedance of the VCO and the input impedance of the PLL can be assumed to be real. If this is not the case, it can be made so by putting a series capacitor or inductor to cancel out the imaginary part. It is common for PLLs to have a negative reactance; and in this case, an inductor can be placed in series to cancel this out. Note that inductors tend to add cost, and this is not necessary unless the negative reactance of the PLL is fairly large. With a maximum of two components, the reactances of both the source and the load can be canceled. In the most common case, the impedance of the trace and VCO are both 50 Ω, but the PLL is something different. In this case, it makes most sense to place the impedance matching network as close to the PLL as possible.

Exactly Matching any Two Real Loads at a Fixed Frequency

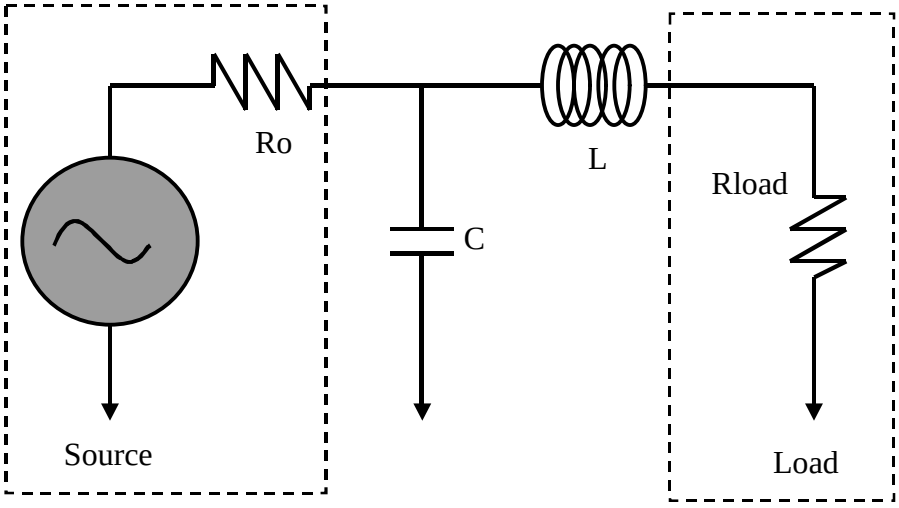


Figure 1 *Typical Impedance Matching Circuit*

For this type of match, the frequency must be specified. Note also that this assumes that the load resistance is greater than the source resistance. If this is not the case, then the inductor L, needs to be moved to the left hand side of capacitor ***C***, instead of the right hand side and the values for the load and source resistance need to be switched. The matching circuit is designed so that both the load and source see a matching impedance. This yields a system of two equations and two unknowns that can be calculated ***L*** and ***C***. In the case that the load has a negative reactance and also has less resistance than the source, it is convenient to compensate for the negative reactance by making the inductor, ***L***, bigger by the appropriate amount.

$$\frac{Ro}{1+s \bullet C \bullet Ro} + s \bullet L = Rload$$

$$\frac{s \bullet L + Rload}{s^2 \bullet L \bullet C + s \bullet Rload \bullet C + 1} = Ro$$

Solving these simultaneous equations yields the following:

$$C = \frac{\sqrt{\frac{Ro}{Rload} - 1}}{w \bullet Ro}$$

$$L = C \bullet Ro \bullet Rload$$

The Resistive Pad

Although the method in the previous section can match any load to any source exactly, it is often not used because inductors are expensive. Also this method is only designed for a fixed frequency and PLL input impedance. If the input impedance of the load varies drastically, then this network will become unoptimized. The resistive pad is a method of matching that does not match exactly, but is very good at accounting for variations in impedance. The biggest disadvantage of the resistive pad is that VCO power must be sacrificed. As more VCO power is sacrificed, the matching ability of the pad increases.

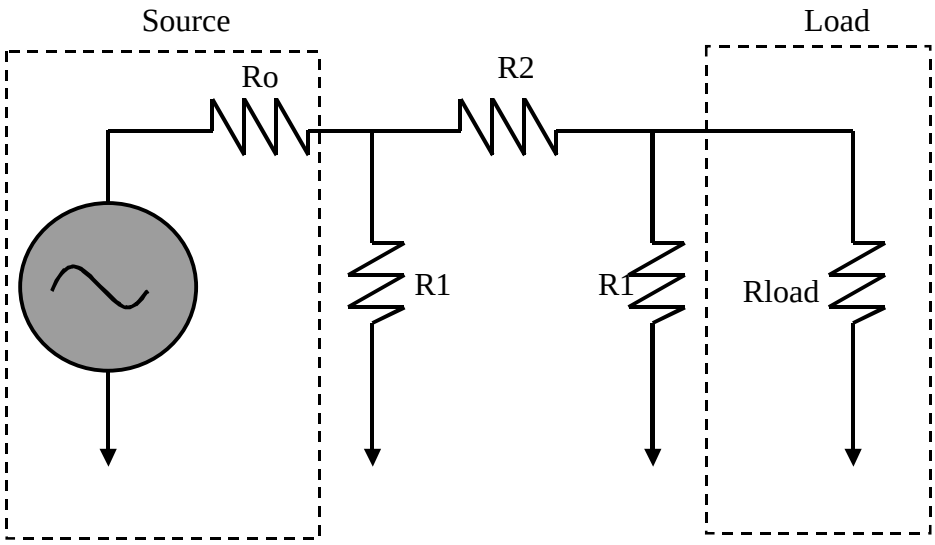


Figure 2 *Typical Resistive Pad*

For the resistive pad, the attenuation of the pad is specified, and it is designed assuming that both the source and load impedance are equal to ***Ro***, usually 50 Ω. The resistor values satisfy the following equations.

$$R1 \| (R2 + R1 \| Ro) = Ro$$

$$\frac{(R1 \| Ro) \bullet R1}{R1 + R2 + R1 \| Ro} = 10^{\frac{Atten}{20}} = K$$

In these equations, ***Ro*** is the source impedance, ***Atten*** is the attenuation of the pad, and ***x*** || ***y*** is used to denote the parallel combination of two components, ***x*** and ***y***. The components ***R1*** and ***R2*** can be calculated as follows:

$$R1 = Ro \bullet \frac{K+1}{K-1}$$

$$R2 = \frac{2 \bullet Ro \bullet R1}{R1^2 - Ro^2}$$

Adjusting the Trace Width to Match the PLL Input Impedance and Keeping Traces Short

Regardless of whether a resistive pad or LC matching network is used, the idea was to make the load impedance look the same as the source impedance. If these impedances are matched, then the trace impedance can be made equal to these impedances, and there will theoretically be no undesired transmission line effects, such as standing waves. Another matching strategy is to match the trace impedance to the PLL input impedance, instead of the VCO output impedance. The matching of the trace impedance to the PLL impedance is much more important than the matching of the trace impedance to VCO output impedance. Also, if the trace is short ($1/10^{th}$ of a wavelength or less), then transmission line effects are much less likely to be present.

Conclusion

Although impedance matching networks are often unnecessary for matching the PLL to the VCO, there are enough situations where they are needed. Actually, what is really more critical is that the PLL input impedance be matched to the characteristic impedance of the PCB trace. When the trace length between the VCO and PLL approaches one-tenth of a wavelength, the trace is considered long and undesired transmission line effects can result. If there is plenty of VCO power to spare, the resistive pad serves as an economical and process-resistant solution. Otherwise, if the PLL is grossly mismatched to the VCO, the approach with inductors and capacitors can provide a good match. When using any sort of matching network, it is important to put this network as close to the PLL as possible.

References

[1] Online Microstrip Impedance Calculator Tool
http://www.emclab.umr.edu/pcbtlc/microstrip.html

[2] Danzer, Paul (editor) *The ARRL Handbook (Chapter 19)* The American Radio Relay League. 1997

17. Routh Stability for PLL Loop Filters

Introduction

There are two ways to make a loop filter unstable. The first is to design for a loop bandwidth that is more than about 1/3rd of the comparison frequency. The second is to design a loop filter such that the poles of the closed loop system fall in the right hand plane. This can happen when the phase margin is too low, at least for a third order filter. For the purposes of this chapter, the term Routh stability refers to a system where all the poles of the closed loop transfer function are in the left hand plane. This chapter examines what restrictions Routh's Stability Criterion implies.

Calculation of Stability Coefficients

The open loop transfer function for a third order filter is as follows:

$$G(s)=\frac{N \bullet K \bullet (1+s \bullet T2)}{s^2 \bullet (1+s \bullet T1) \bullet (1+s \bullet T3)}$$

$$K=\frac{Kf \bullet Kvco}{N \bullet (C1+C2+C3)}$$

The closed loop transfer function is as follows:

$$\frac{G(s)}{1+G(s)/N}=\frac{N \bullet K \bullet (1+s \bullet T2)}{s^4 \bullet d4+s^3 \bullet d3+s^2 \bullet d2+s \bullet d1+d0}$$

The constants in the denominator are the stability coefficients that determine the stability of the system and are defined as follows:

$$d4 = T1 \bullet T3$$
$$d3 = T1+T3$$
$$d2 = 1$$
$$d1 = T2 \bullet K$$
$$d0 = K$$

Formation of a Routh Table

The system will be stable if all of the poles of the denominator have negative real parts. Instead of explicitly calculating the roots, it is far easier to use Routh's stability criterion, which says that all the roots have negative real parts if and only if the elements in the Routh array are positive. The elements in the Routh Array are the elements in the second column of the Routh table that is shown below. The Routh table is formed by putting the odd terms in the first row and the even terms in the second row. Note that the term with the highest power is considered to be the first term, and therefore an odd term. The lower rows are formed by taking the determinant of the 2 X 2 matrix formed by eliminating the column that the entry of interest is in, and dividing by the first entry in the row above the entry of interest. This is shown in Table 1.

s^n	d_n	d_{n-2}	d_{n-4}	…
s^{n-1}	d_{n-1}	d_{n-3}	d_{n-5}	…
	$b_1 = \frac{d_{n-1} \bullet d_{n-2} - d_n \bullet d_{n-3}}{d_{n-1}}$	$b_2 = \frac{d_{n-1} \bullet d_{n-4} - d_n \bullet d_{n-5}}{d_{n-1}}$	…	…
	$c_1 = \frac{b_1 \bullet d_{n-2} - b_2 \bullet d_n}{b_1}$	…	…	…

Table 1 *A Generic Routh Table*

Proof of Routh Stability for a Second Order Filter

The second order loop filter is a special case of the third order loop filter in which ***T3 = 0***. The Routh table for the second order filter is shown below:

s^3	*T1*	*T2•K*
s^2	*1*	*K*
	K•(T2 – T1)	*0*
	K	*0*

Table 2 *Routh Table for Second Order Loop Filter*

Now from the definition of ***K***, it is clear that ***K>0***. From the third row, this puts the restriction that ***T2 > T1***. For a second order filter, this is always the case because:

$$T2 = R2 \bullet C2$$

$$T1 = T2 \bullet \frac{C1}{C1 + C2}$$

Theorem 1:

Using real component values and the standard loop filter topology, it is impossible to design a second order loop filter which is unstable, provided that the loop bandwidth is sufficiently small to justify the continuous time approximation.

So using the standard topology, it is impossible to design a loop filter that is unstable due to too low phase margin or poles in the right hand plane. This stability makes the second order filter a good choice when the VCO gain, charge pump gain, or N value drastically varies.

Conditions for Third Order Routh Stability

For the third order filter, it turns out that the Routh table is not so simple and that it is possible to design an unstable loop filter, regardless of loop bandwidth. Since the loop bandwidth decreases as the charge pump gain or VCO gain decreases, reducing these will eventually guarantee second order filter stability, and will always make a third order filter stable provided ***T2 > T1 + T3***. For the purposes of simplifying the math in the Routh table, the following constant is introduced.

$$c = \frac{T1 + T3}{T1 \bullet T2 \bullet T3}$$

s^4	$T1 \bullet T3$	1	K
s^3	$T1 + T3$	$T2 \bullet K$	0
	$1 - K/c$	K	0
	$\dfrac{\frac{K \bullet T2}{c} \bullet \left[\frac{T2 - T1 - T3}{T2} \bullet c - K\right]}{1 - K/c}$	0	0
	K		

Table 3 *Third Order Routh Stability Table*

Substituting the definitions in for the constants ***c*** and ***K***, and also using the leading elements in the third and fourth rows yields the constraints for third order filter stability:

$$\frac{Kf \bullet Kvco}{N \bullet (C1+C2+C3)} < \frac{T1+T3}{T1 \bullet T2 \bullet T3}$$

$$\frac{Kf \bullet Kvco}{N \bullet (C1+C2+C3)} < \frac{T1+T3}{T1 \bullet T2 \bullet T3} \bullet \frac{T2-T1-T3}{T2}$$

However, these first constraint is redundant; therefore, the criteria for third order stability is:

$$\frac{Kf \bullet Kvco}{N \bullet (C1+C2+C3)} < \frac{T1+T3}{T1 \bullet T2 \bullet T3} \bullet \frac{T2-T1-T3}{T2}$$

This criteria implies that $T2 > T1 + T3$.

Conclusion

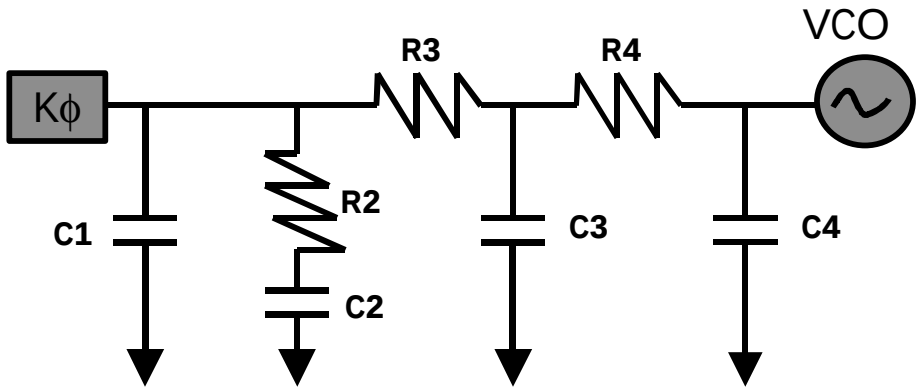
The conditions for stability of loop filters have been investigated. There is always the condition that the loop bandwidth be sufficiently narrow relative to the comparison frequency, but there is also the constraint that all the poles of the closed loop transfer function have negative real parts. For the second order filter, this was shown to always be the case, but for the third, there were real restrictions. The fourth order filter was not covered in this chapter, since its Routh Table is rather complicated in the general case. However, similar restrictions on the time constants, VCO gain, and charge pump gain exist for the fourth order filter.

This chapter was actually inspired by the quest to find a filter that attenuated the spurs more. Notice that ***T2*** must be larger than ***T1*** or ***T3*** for the PLL to be stable. Theoretically, if ***T3*** or ***T1*** is chosen larger than ***T2***, then the spurs could be reduced significantly. This chapter on Routh Stability proves why this type of loop filter will never be stable. The zero ***T2*** is necessary for stability because of the ***1/s*** factor introduced by the VCO.

References

Franklin, G., et. al. *Feedback Control of Dynamic Systems* Addison Wesley

18. A Sample Loop Filter Analysis



ENTER PARAMETERS HERE

$K\phi := 5 \cdot mA$ $Fcomp := 200kHz$ $Fout := 900MHz$ $Kvco := 20\frac{MHz}{volt}$

$C1 := 4 \cdot nF$ $C2 := 100nF$ $C3 := 1000pF$ $C4 := 100pF$

$R2 := 1 \cdot k\Omega$ $R3 := 2 \cdot k\Omega$ $R4 := 2 \cdot k\Omega$

CALCULATE PARAMETERS

$$N := \frac{Fout}{Fcomp} \qquad N = 4.500 \times 10^{3}$$

DEFINE LOOP PARAMETERS

$a := R2 \cdot R3 \cdot R4 \cdot C1 \cdot C2 \cdot C3 \cdot C4$ $d := C1 + C2 + C3 + C4$

$b := C1 \cdot C2 \cdot R2 \cdot R3 \cdot (C3 + C4) + R4 \cdot C4 \cdot (C2 \cdot C3 \cdot R3 + C1 \cdot C3 \cdot R3 + C1 \cdot C2 \cdot R2)$

$c := R2 \cdot C2 \cdot (C1 + C3 + C4) + R3 \cdot (C1 + C2) \cdot (C3 + C4) + R4 \cdot C4 \cdot (C1 + C2 + C3)$

$$Z(s) := \frac{1 + R2 \cdot C2 \cdot s}{s \cdot (a \cdot s^3 + b \cdot s^2 + c \cdot s + d)}$$ Loop Filter Impedance

$$G(s) := \frac{K\phi \cdot Kvco \cdot Z(s)}{s}$$ Forward Loop Gain

$$CL(s) := \frac{G(s)}{1 + \frac{G(s)}{N}}$$ Closed Loop Gain

BANDWIDTH AND PHASE MARGIN

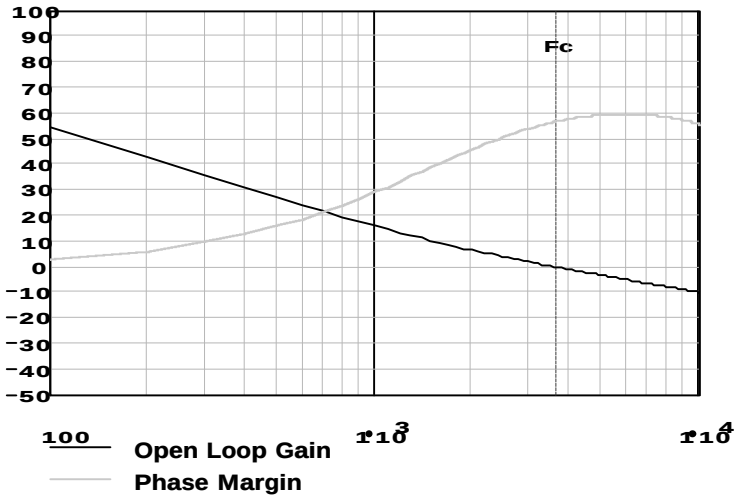
$Fc := root(|G(x \cdot 2\cdot\pi\cdot i)| - N, x)$ $Fc = 3.641\,kHz$ Loop Bandwidth

$f := Fc$

$arg(G(Fc\cdot 2\cdot\pi\cdot i))\cdot\frac{180}{\pi} + 180 = 56.953$ Phase Margin

DISPLAY BODE PLOT

$x := 1\cdot Hz, 100\cdot Hz .. 50\cdot Fc$ Open Loop Gain and Phase Margin



CALCULATE OPTIMIZATION INDEX

$k := 1 .. 1000$

$x_k := arg\left(G\left(\frac{2\cdot Fc}{1000}\cdot k\cdot 2\cdot\pi\cdot i\right)\right)\cdot\frac{180}{\pi} + 180$

$\left(\frac{arg(G(Fc\cdot 2\cdot\pi\cdot i))\cdot\frac{180}{\pi} + 180}{max(x)}\right)^4 = 82.720\%$ Optimization Index

Note here that the optimization index is the ratio of the phase margin divided by the maximum value that this function achieves. The power that it is raised to is arbitrary. A perfectly optimized filter will have an optimization index of 100%. For a second order filter, simulations show that choosing the optimization index to be 100% yields the fastest possible lock time. However, for third and higher order filters, simulations show that this is not exactly the criterion for optimal lock time, although it is a good rule of thumb.

CALCULATE THE TRUE POLES AND ZERO

$T2 := R2 \cdot C2$

$A := \frac{a}{d} \qquad B := \frac{b}{d} \qquad C := \frac{c}{d}$

$C = 7.226 \cdot 10^{-6} \cdot \text{sec}$

$r := \text{polyroots}\left(\begin{bmatrix} -A \cdot A \cdot \text{sec}^{-6} \\ A \cdot C \cdot \text{sec}^{-4} \\ -B \cdot \text{sec}^{-2} \\ 1 \end{bmatrix}\right) \cdot \text{sec}^2 \qquad r = \begin{bmatrix} 2.735 \cdot 10^{-13} \\ 1.030 \cdot 10^{-12} \\ 8.226 \cdot 10^{-12} \end{bmatrix} \cdot \text{sec}^2$

$T1 := \frac{A}{\min(r)}$

$r := \text{polyroots}\left(\begin{bmatrix} \min(r) \cdot \text{sec}^{-2} \\ (T1 - C) \cdot \text{sec}^{-1} \\ 1 \end{bmatrix}\right) \cdot \text{sec} \qquad r = \begin{bmatrix} 1.854 \cdot 10^{-7} \\ 1.476 \cdot 10^{-6} \end{bmatrix} \cdot \text{sec}$

$T3 := \max(r) \qquad T4 := \min(r)$

Time Constant	ter Pole	Filter Zero
$T1 = 5.566 \cdot 10^{-6} \cdot \text{sec}$	$\frac{1}{T1} = 179.650 \cdot \text{kHz}$	n/a
$T2 = 1.000 \cdot 10^{-4} \cdot \text{sec}$	n/a	$\frac{1}{T2} = 10.000 \cdot \text{kHz}$
$T3 = 1.476 \cdot 10^{-6} \cdot \text{sec}$	$\frac{1}{T3} = 676.651 \cdot \text{kHz}$	n/a
$T4 = 1.854 \cdot 10^{-7} \cdot \text{sec}$	$\frac{1}{T4} = 5.404 \cdot 10^{6} \cdot \text{sec}^{-1}$	n/a

Pole Ratios

$\frac{T3}{T1} = 26.550\%$ $\qquad \frac{T4}{T1} = 3.325\%$ $\qquad \frac{T4}{T3} = 12.522\%$

The calculation of the zero, ***T2***, is very easy. However, the calculation of the poles can be more involved. In order to solve for them, it is necessary to set up a system of three equations and three unknowns, which requires that a cubic polynomial be solved. This system comes from equating the coefficients in the loop filter impedance. In the case of a third order filter, the system is reduced to two equations and two unknowns, which requires a quadric polynomial to be solved. In the case of a second order filter, the pole can be directly solved for.

PHASE NOISE PROFILE

$Noise1Hz := -213$ dbc/Hz

1 Hz Normalized Phase Detector Noise
LMX2330, Aux side powered down,
High charge pump gain setting

$$NoiseFloor := Noise1Hz + 10\log\left(\frac{Fcomp}{Hz}\right)$$

$NoiseFloor = -159.990$ dbc/Hz

Noise Floor of PLL

$$PLLNoise(f) := NoiseFloor + 20\log\left(\left|CL(f \cdot 2 \cdot \pi \cdot i)\right|\right)$$

$PLLNoise(150Hz) = -86.889$

Close In Phase Noise

VCO Noise

$VCO10khz := -100$ dbc/Hz

$$VCONoise(f) := VCO10khz - 20\log\left(\frac{f}{10kHz}\right) - 20\log\left(\left|1 + \frac{G(f \cdot 2 \cdot \pi \cdot i)}{N}\right|\right)$$

Resistor Noise Properties

$k := 1.3806503 \cdot 10^{-23} \cdot \frac{joule}{K}$ $\quad T_o := 300K$ $\quad R\_Noise(R) := \sqrt{4 \cdot T_o \cdot k \cdot R \cdot 1 \cdot Hz}$

R2 Resistor Noise

$VnR2 := R\_Noise(R2)$ $\quad VnR2 = 4.070 \cdot 10^{-9} \cdot volt$

$$Z1(s) := \frac{1}{s \cdot C2} + R2$$

$$Z(s) := \frac{1}{s \cdot (C1 + C3 + C4 + s \cdot (C3 \cdot C4 \cdot R4 + C3 \cdot R3 \cdot C1 + C4 \cdot R4 \cdot C1 + R3 \cdot C4 \cdot C1) + s^2 \cdot C1 \cdot C3 \cdot C4 \cdot R3 \cdot R4)}$$

$$TR2(s) := \left|\frac{1}{1 + \frac{G(s)}{N}}\right| \cdot \left|\frac{Z1(s)}{Z1(s) + Z(s)}\right|$$

$$R2\_Noise(f) := 20\log\left(\left|\frac{\sqrt{2} \cdot VnR2 \cdot TR2(2 \cdot \pi \cdot i \cdot f) \cdot Kvco}{2 \cdot f}\right|\right)$$

R3 Resistor Noise

$VnR3 := R\_Noise(R3)$ $\quad VnR3 = 5.756 \cdot 10^{-9}\ volt$

$$Z1(s) := \frac{1 + s \cdot C2 \cdot R2}{s \cdot (C1 + C2) + s^2 \cdot C1 \cdot C2 \cdot R2} + R3 \qquad Z2(s) := \frac{1 + s \cdot C4 \cdot R4}{s \cdot C3 + s \cdot C4 + s^2 \cdot C3 \cdot C4 \cdot R4}$$

$$TR3(s) := \frac{1}{\left| 1 + \frac{G(s)}{N} \right|} \cdot \left| \frac{Z1(s)}{Z1(s) + Z2(s)} \cdot \frac{1}{1 + s \cdot C4 \cdot R4} \right|$$

$$R3\_Noise(f) := if\left(R3 > 1 \cdot \Omega\ ,\ 20 \log\left(\left| \frac{\sqrt{2} \cdot VnR3 \cdot TR3(2 \cdot \pi \cdot i \cdot f) \cdot Kvco}{2 \cdot f} \right| \right), -500 \right)$$

R4 Resistor Noise

$VnR4 := R\_Noise(R3)$ $\quad VnR4 = 5.756 \cdot 10^{-9}\ volt$

$$Z2(s) := \frac{1 + s \cdot C2 \cdot R2}{s \cdot (C1 + C2) + s^2 \cdot C1 \cdot C2 \cdot R2} \qquad Z(s) := R4 + \frac{R3 + Z2(s)}{1 + s \cdot C3 \cdot R3 + s \cdot C3 \cdot Z2(s)}$$

$$TR4(s) := \frac{1}{\left| 1 + \frac{G(s)}{N} \right|} \cdot \left| \frac{1}{1 + s \cdot C4 \cdot Z(s)} \right|$$

$$R4\_Noise(f) := if\left(R4 > 1 \cdot \Omega\ ,\ 20 \log\left(\left| \frac{\sqrt{2} \cdot VnR4 \cdot TR4(2 \cdot \pi \cdot i \cdot f) \cdot Kvco}{2 \cdot f} \right| \right), -500 \right)$$

Reference Spur Simulation

User Enters These

LeakageSpur_00 := 16.0 dbc — This is a universal empirical constant

LeakageCurrent := 10^{-9} amp — Enter the leakage current of the PLL

PulseSpur_00 := −311 dbc — This is a part-specific constant

Modulo := 1 — Fractional Modulus, enter '1' for Integer PLL

Calculations

$$Fspur := \frac{Fcomp}{Modulo}$$

$$SpurGain := 20\log\left(\left|G(Fspur \cdot 2\cdot\pi\cdot i)\right|\right) \qquad SpurGain = 13.889$$

$$LeakageSpur := LeakageSpur\_00 - 20\log\left(\frac{LeakageCurrent}{K_\phi}\right) + SpurGain$$

$$PulseSpur := PulseSpur\_00 + SpurGain + 40\log\left(\frac{Fspur}{1\cdot Hz}\right)$$

$$TotalSpur(f) := if\left(\left|f - Fspur\right| < 100Hz,\ 10\log\left(10^{\frac{PulseSpur}{10}} + 10^{\frac{LeakageSpur}{10}}\right),\ -500\right)$$

Spur Due to Leakage	Spur Due to Pulse	Composite Spur
LeakageSpur = −104.090	PulseSpur = −85.070	TotalSpur(Fspur) = −85.016

Although it is possible to make some intelligent estimates of the reference spur levels, there will always be some variation between the estimated levels and the simulated levels. Note also that the spur level displayed is what is expected when the VCO tuning voltage is varied 0.5 volts from the power supply rails.

Total Noise Properties

$$TotalNoise(f) := 10\log\left(10^{\frac{PLLNoise(f)}{10}} + 10^{\frac{VCONoise(f)}{10}} + 10^{\frac{R2\_Noise(f)}{10}} + 10^{\frac{R3\_Noise(f)}{10}} + 10^{\frac{R4\_Noise(f)}{10}} + 10^{\frac{TotalSpur(f)}{10}}\right)$$

$$10^{\frac{VCO10kHzNoiseFloor - 20\log(N)}{20}} \cdot 10\,kHz = 2.220\,kHz$$ Min RMS Bandwidth

$$\sqrt{2 \cdot sec \cdot \int_{100\,Hz}^{15\,kHz} 10^{\frac{TotalNoise(f)}{10}}\,d\omega} = 0.405\,deg$$ RMS Phase Error

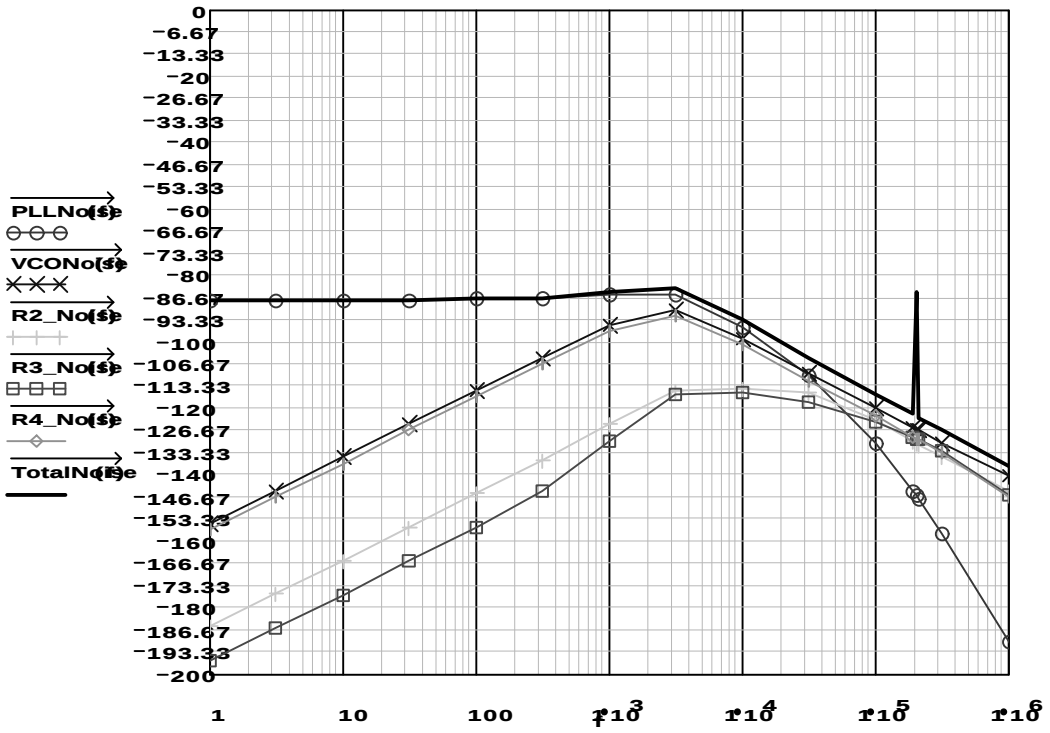
Simulated Spectrum Analyzer

$span := 5 \cdot Fcomp$ Enter the Span in kHz

Phase Noise/Spurs at Various Offsets

$TotalNoise(100\,Hz) = -86.897$ dbc/Hz Close-in Phase Noise

$TotalSpur(Fspur) = -85.016$ dbc First Reference Spur (Worst Case)



Note

TRANSIENT ANALYSIS

User Enters these

$f2 := 905MHz$ Final Frequency — N value for f2

$f1 := 895MHz$ Starting Frequency

$tol := 1000Hz$ Tolerance for Lock Time Measurments

Calculations

$$R3 := \max\left(\begin{bmatrix} R3 \\ 1\cdot\Omega \end{bmatrix}\right) \qquad C3 := \max\left(\begin{bmatrix} C3 \\ 1\cdot pF \end{bmatrix}\right) \qquad N := \frac{f2}{Fcomp}$$

$$den2 := C1 + C2 + C3$$

$$den4 := R2\cdot R3\cdot C1\cdot C2\cdot C3 \qquad den3 := C2\cdot C3\cdot R2 + C1\cdot C2\cdot R2 + C1\cdot C3\cdot R3 + C2\cdot C3\cdot R3$$

$$den1 := \frac{K\phi\cdot Kvco\cdot C2\cdot R2}{N} \qquad num0 := \frac{K\phi\cdot Kvco\cdot(f2 - f1)}{N}$$

$$den0 := \frac{K\phi\cdot Kvco}{N} \qquad num1 := num0\cdot R2\cdot C2$$

$$v := \begin{bmatrix} \frac{den0}{den4}\cdot sec^{4} \\ \frac{den1}{den4}\cdot sec^{3} \\ \frac{den2}{den4}\cdot sec^{2} \\ \frac{den3}{den4}\cdot sec \\ 1 \end{bmatrix} \qquad v = \begin{bmatrix} 2.762\cdot10^{19} \\ 2.762\cdot10^{15} \\ 1.312\cdot10^{11} \\ 8.850\cdot10^{5} \\ 1.000 \end{bmatrix}$$

$$p := polyroots(v)\cdot sec^{-1} \qquad p = \begin{bmatrix} -7.044\cdot10^{5} \\ -1.580\cdot10^{5} \\ -1.145\cdot10^{4} + 1.082\cdot10^{4}\,i \\ -1.145\cdot10^{4} - 1.082\cdot10^{4}\,i \end{bmatrix}\cdot sec^{-1}$$

These are the poles

$$A_0 := \frac{\frac{num0}{den4}}{(p_0 - p_1)\cdot(p_0 - p_2)\cdot(p_0 - p_3)} \qquad A_0 = -1.054\cdot10^{9}\cdot sec^{-2}$$

$$A_1 := \frac{\frac{num0}{den4}}{(p_1 - p_0)\cdot(p_1 - p_2)\cdot(p_1 - p_3)} \qquad A_1 = 2.342\cdot10^{10}\cdot sec^{-2}$$

$$A_2 := \frac{\frac{num0}{den4}}{(p_2 - p_0)\cdot(p_2 - p_1)\cdot(p_2 - p_3)} \qquad A_2 = -1.116\cdot10^{10} - 1.249\cdot10^{11}i \cdot sec^{-2}$$

$$A_3 := \frac{\frac{num0}{den4}}{(p_3 - p_0)\cdot(p_3 - p_1)\cdot(p_3 - p_2)} \qquad A_3 = -1.116\cdot10^{10} + 1.249\cdot10^{11}i \cdot sec^{-2}$$

4 Pole Analysis

$k := 0..5000$ $\quad t_k := \frac{k}{1000000}\cdot sec$

$i := 0..3$

$$F(t) := f2 + \sum_i A_i \cdot e^{p_i \cdot t_k}\left(\frac{1}{p_i} + R2\cdot C2\right)$$

Enter these to adjust the setting

$range := 5000\cdot10^{(-6)}\cdot sec$ Maximum Range of the X axis

$span := 0.01MHz$ Vertical Span of the Plot

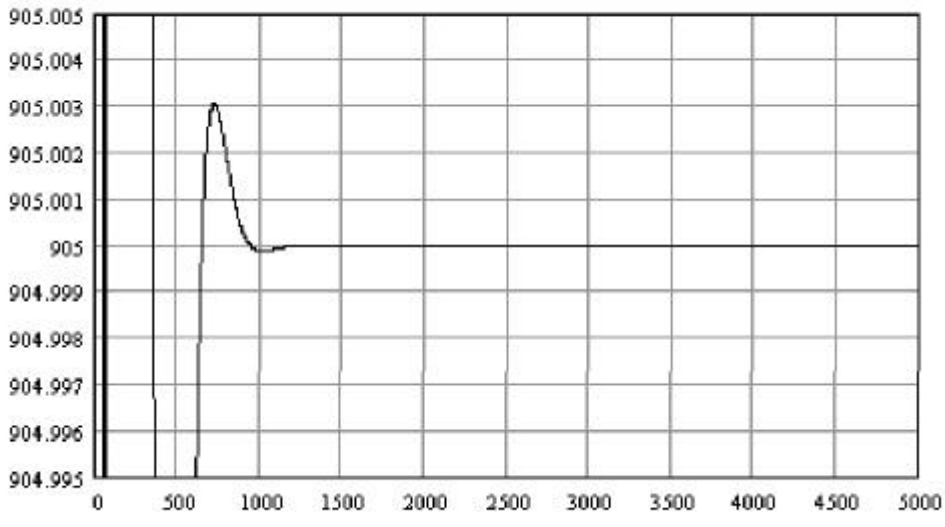
$center := 905MHz$ Center Frequency

PLL Transient Response

$LockTime = 841.000\,\mu sec$ Lock Time in microseconds

$OverShoot = 10.003MHz$ Amount frequency overshoot

$tol = 1.000\cdot10^{3}\cdot Hz$ Frequency Tolerance



Conclusion

This chapter has presented the analysis of the loop filter using concepts presented in previous chapters.

19. Basic Prescaler Operation

Introduction

Until now, the N counter has been treated as some sort of black box that divides the VCO frequency and phase by N. It could be implemented with a digital counter fabricated with a low frequency process, such as CMOS, if the output frequency of the VCO is low (200 MHz or less). However, if the VCO frequency is much higher than this, then a pure CMOS counter is likely to have difficulty dealing with the higher frequency. It is desirable to implement as much of the N counter in CMOS as possible, for lower cost and current consumption. To resolve this dilemma, prescalers are often used to divide down the VCO frequency to something that can be handled with lower the frequency processes. Prescalers often divide by some power of two, since this makes them easier to implement. The most common implementations of prescalers are single modulus, dual modulus, and quadruple modulus. Of these, the dual modulus prescaler is most commonly used.

Single Modulus Prescaler

For this approach, a single high frequency divider placed in front of a counter. In this case, $\boldsymbol{N = a \bullet P}$, where $\boldsymbol{a}$ can be changed and $\boldsymbol{P}$ is fixed. One disadvantage of this prescaler is that only N values that are an integer multiple of $\boldsymbol{P}$ can be synthesized. Although the channel spacing can be reduced to compensate for this, doing so increases phase noise substantially. This approach also is popular in high frequency designs (>3 GHz) in which a fully integrated PLL can not be fabricated totally in silicon. In this case, divide by two prescalers made with the GaAs or SiGe process can be used in conjunction with a PLL. Single modulus prescalers are also sometimes used in older PLLs and low cost PLLs.

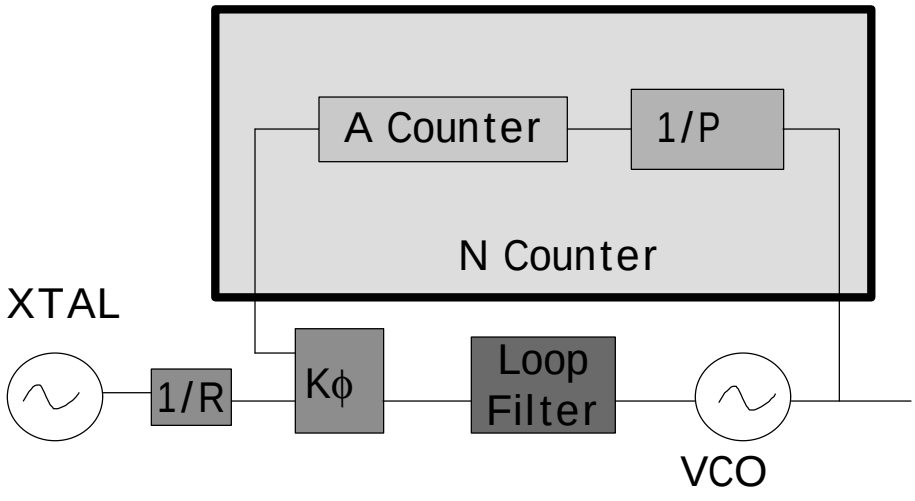


Figure 1 *Single Modulus Prescaler*

Dual Modulus Prescaler

In order not to sacrifice frequency resolution, a dual modulus prescaler is often used. These come in the form ***P/(P+1)***. For instance, a ***32/33*** prescaler has ***P = 32***. At first a fixed prescaler of size ***P+1***, which is actually a prescaler of size ***P*** with a pulse swallow circuit, is engaged for a total of ***a*** cycles. Since the A counter activates the pulse swallow circuitry, it is often referred to as the swallow counter. It takes a total of ***a•(P+1)*** cycles for the A counter to count down to zero. Then the B counter starts counting down. Since it started with ***b*** counts, the remaining counts would be (***b – a)***. The size P prescaler is then switched in. This takes ***(b-a)•P*** counts to finish up the count, at which time, all of the counters are reset, and the process is repeated.

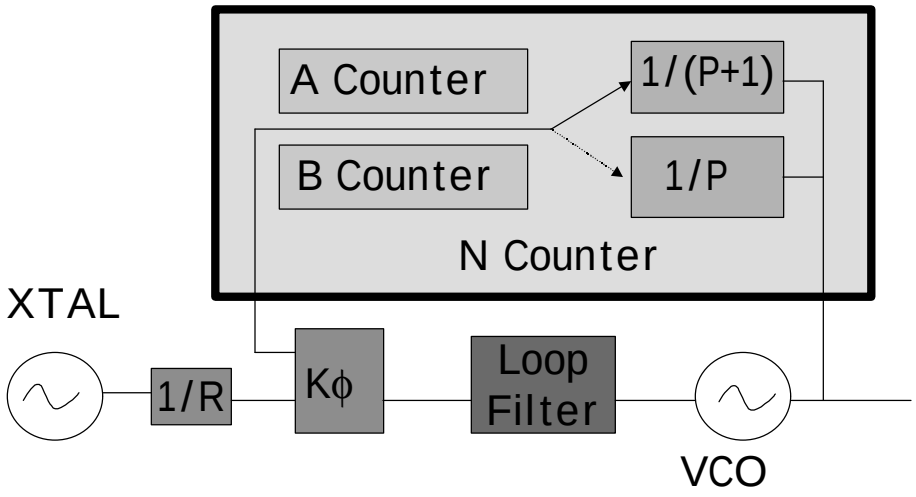


Figure 2 *Dual Modulus Prescaler*

Notice that ***b>=a***, in order for proper operation, otherwise the B counter would prematurely reach zero and reset the system. For this reason, N values that yield ***b<a*** are called illegal divide ratios. From this we get the fundamental equations:

$$N = (P+1)\bullet a + P\bullet(b-a) = P\bullet b + a$$

$$b = N \text{ div } P \qquad \text{(N divided by P, disregarding the remainder)}$$

$$a = N \bmod P \qquad \text{(The remainder when N is divided by P)}$$

Note that this prescaler gains better resolution at the cost of not being able to synthesize all N values. If the N value is greater or equal to ***P•(P-1)***, then the condition that ***b>=a*** is automatically satisfied. The lower bound, ***L***, such that all N values are legal provided ***N>=L*** is referred to as the minimum continuous divide ratio.

Quadruple Modulus Prescalers

In order to achieve a lower minimum continuous divide ratio, the quadruple modulus prescaler is often used. In the case of a quadruple modulus prescaler, there are four prescalers, but only three are used to produce any given N value. Commonly, these four prescalers are of values ***P***, ***P+1***, ***P+4***, and ***P+5***, and are implemented with a single pulse swallow circuit and a four-pulse swallow circuit. The N value produced is:

$$N = P \bullet c + 4 \bullet b + a$$

$$a = N \bmod P$$

$$c = N \operatorname{div} P$$

$$b = \frac{N - c \bullet P - a}{4}$$

The following table shows the three steps and how the prescalers are used in conjunction to produce the required N value. Regardless of whether or not ***b*>=*a***, the resulting N value is the same. Note that the ***b*>=*a*** restriction applies to the dual modulus prescaler, but not the quadruple modulus prescaler. The restriction for the quadruple modulus prescaler is ***c* >= *max{ a, b }***.

	If b>=a		If b<a	
Step	**Description**	**Counts Required**	**Description**	**Counts Required**
1	The P+5 prescaler is engaged in order to decrement the A counter until a=0.	a●(P+5)	The P+5 prescaler is engaged in order to decrement the B counter until b=0.	b● (P+5)
2	The P+4 prescaler is engaged in order to decrement the B counter until b=0.	(b-a)●(P+4)	The P+1 prescaler is engaged in order to decrement the A counter until a=0.	(a-b)●(P+1)
3	The P prescaler is engaged in order to decrement the C counter until c=0.	(c-b)●P	The P prescaler is engaged in order to decrement the C counter until c=0.	(c-a)●P
	Total Counts	P●c+4●b+a	Total Counts	P●c+4●b+a

Table 1 *Typical Operation of a Quadruple Modulus Prescaler*

Conclusion

For PLLs that operate at higher frequencies, prescalers are necessary to overcome process limitations. The basic operation of the single, dual, and quadruple modulus prescaler has been presented. Prescalers combine with the A, B, and C counters in order to synthesize the desired N value. For all prescalers, not all N values are possible there will be N values that are unachievable. The advantage of using higher modulus prescalers is that a greater range of N values can be achieved, particularly the lower N values. Many PLLs allow the user more than one choice of prescaler to use. In the case of an integer PLL, the prescaler used usually has no impact on the phase noise, reference spurs, or lock time. This is assuming that the N value is the same. For some fractional N PLLs the choice of prescaler may impact the phase noise and reference spurs, despite the fact that the N value is unchanged.

20. Fundamentals of Fractional N PLLs

Introduction

One popular misconception regarding fractional N PLLs is that they require different design equations and simulation techniques than are used for integer N PLLs. This is not true. However, since fractional N PLLs contain compensation circuitry for the fractional spurs, they may exhibit some behaviors that would not be expected from an integer PLL. In addition to this, the performance will also be different, due to the fact that the N value is different. This chapter discusses some of the theoretical and practical behaviors of fractional N PLLs.

Theoretical Explanation of Fractional N

Fractional N PLLs differ from integer N PLLs in that some fractional N values are permitted. In general, a modulo M fractional N PLL allows N values in the form of $N + \frac{i}{M}$, where N is the integer portion, ***i*** ranges from 0 to ***M-1***, and ***M*** is the fractional Modulus. Because the N value can now be a fraction, this allows the comparison frequency to be increased by a factor of ***M***, while still retaining the same channel spacing.

However, there could be other restrictions, such as illegal divide ratios, maximum phase detector frequency limits, or the crystal frequency, that could prevent the comparison frequency from being increased by a factor of M. Illegal divide ratios can become a barrier to using a fractional N PLL, because reducing the N value may cause it to be an illegal divide ratio. Decreasing the N value corresponds to increasing the phase detector rate, which still must not exceed the maximum value in the datasheet specification. The crystal can also limit the use of fractional N, since the R value must be an integer. This implies that the crystal frequency must be a multiple of the comparison frequency.

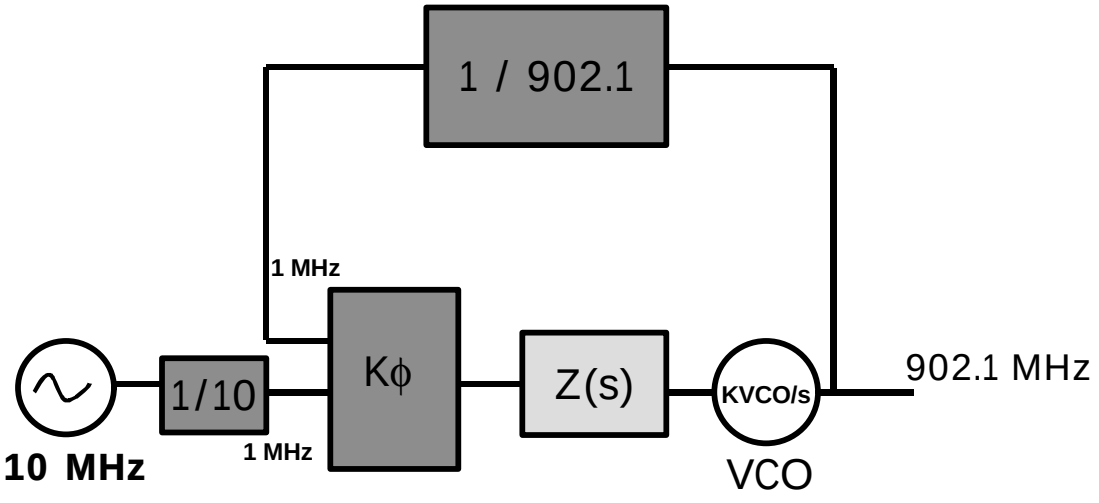


Figure 1 *Fractional N PLL Example*

Figure 1 shows an example of a fractional N PLL generating 902.1 MHz with ***M=10***. This PLL has a channel spacing of 100 KHz, but a reference frequency of 1 MHz. Now assume that the PLL tunes from 902 MHz to 928 MHz with a channel spacing of 100 KHz. The N value

therefore ranges from 902.0 – 928.0. If a 32/33 dual modulus prescaler and the crystal frequency is 10 MHz was used, the R counter value would be an integer and all N values would be legal divide ratios. In this case, the crystal frequency and prescaler did restrict the use of fractional N. Now assume that this PLL of fractional modulus of ***M*** is to be used and the PLL phase detector works up to 10 MHz. Below is a table showing if and how a modulo ***M*** PLL could be used for this application. Since the comparison frequency is never bigger than 1600 MHz, there is no problem with the 10 MHz phase detector frequency limitation. In cases where the prescaler will not work, suggested values are given that will work. Since the quadruple modulus prescaler is able to achieve lower minimum continuous divide ratios, they tend to be more common in fractional N PLLs than integer N PLLs.

Fractional Modulo	Comparison Frequency	32/33 Prescaler Check	Prescaler Suggestion	10 MHz Crystal Check	Crystal Suggestion
1	100 KHz	OK		OK	
2	200 KHz	OK		OK	
3	300 KHz	OK		FAIL	14.4 MHz
4	400 KHz	OK		OK	
5	500 KHz	OK		OK	
6	600 KHz	OK		FAIL	6.0 MHz
7	700 KHz	OK		FAIL	7.0 MHz
8	800 KHz	OK		OK	
9	900 KHz	OK		FAIL	14.4 MHz
10	1000 KHz	FAIL	16/17	OK	
11	1100 KHz	FAIL	16/17	FAIL	11.0 MHz
12	1200 KHz	FAIL	16/17	FAIL	14.4 MHz
13	1300 KHz	FAIL	16/17	FAIL	13.0 MHz
14	1400 KHz	FAIL	16/17	FAIL	14.0 MHz
15	1500 KHz	FAIL	16/17	FAIL	15.0 MHz
16	1600 KHz	FAIL	16/17	FAIL	14.4 MHz

Table 2 *Fractional N Example*

Phase Noise for Fractional N PLLs

Since the N value is lower by a factor of ***M*** (the fractional modulus), one would expect the phase noise to be lower by ***10•log(M)***. However, this analysis disregards the fact that the fractional compensation circuitry can add significant phase noise. A good example is the National Semiconductor LMX2350. Theoretically, using this part in modulo 16 mode, one would expect a theoretical improvement of 12 db over its integer N counterpart, the LMX2330. However, at 3 V, the improvement is closer to 1 db. This is because the fractional circuitry adds about 11 db of noise. Using this part in modulo 8 mode at 3 V would actually yield a degradation of 2 db. However, at 4 V and higher operation, the fractional circuitry only adds 7 db, making this part more worthwhile. Depending on the method of fractional compensation used and the PLL, the added noise due to the fractional circuitry can be different. Many fractional N PLLs also have selectable prescalers, which can have a large impact on phase noise. For an integer part, choosing a different prescaler has no impact on phase noise. Also some parts allow the fractional compensation circuitry to be bypassed, which results in an fair improvement in phase noise at the expense of a large increase in the reference spurs. For some applications, the loop bandwidth may be narrow enough to tolerate the increased reference spurs.

Fractional Spurs for Fractional N PLLs

Since the reference spurs for a fractional N PLL are M times the frequency offset away, they are often not a problem, since the loop filter can filter them more. However, fractional N PLLs also have fractional N spurs, which are caused by imperfections in the compensation circuitry. The first fractional spur is typically the most troublesome and occurs at ***1/M*** times the comparison frequency, which is the same offset that the main reference spur occurs for the integer N PLL. As with phase noise, the fractional spur level is also dependent on the choice of prescaler and voltage. Recall from the reference spur chapter that the ***BasePulseSpur*** for the LMX2350 contains an added term, which depends on the output frequency. If the fractional numerator is set to one, then all the fractional spurs will be present. However, the k^{th} fractional spur will be worst when the fractional numerator is equal to k. It is not necessarily true that switching to a fractional N PLL will better spur levels. Fractional N PLLs have the greatest chance for spur levels when the comparison frequency is low and the spurs in the integer PLL are leakage dominated. Fractional spurs are highly resistant to leakage currents. To confirm this, leakage currents up to 5 μA were induced to a PLL with 25 KHz fractional spurs (***M=16***, ***Fcomp=400 KHz***) and there was no observed degradation in spur levels.

Lock Time for Fractional N PLLs

There are two indirect ways that a fractional N PLL can yield improvements in lock time. The first situation is where the fractional N part has lower spurs, thus allowing an increase in loop bandwidth. If the loop bandwidth is increased, then the lock time can be reduced in this way. The second, and more common, situation occurs when the discrete sampling rate of the phase detector is limiting the loop bandwidth. Recall that the loop bandwidth can not be practically made much wider than $1/5^{th}$ of the comparison frequency. If the comparison frequency is increased by a factor of M, then the loop bandwidth can be increased. This is assuming that the spur levels are low enough to tolerate this increase in loop bandwidth.

Fractional N Architectures

The way that fractional N values are typically achieved is by toggling the N counter value between two or more values, such that the average N value is the desired fractional value. For instance, to achieve a fractional value of 100 1/3, the N counter can be made 100, then 100 again, then 101. The cycle repeats. The simplest way to do the fractional N averaging is to toggle between two values, but it is possible to toggle between three or more values. This technique is referred to as dithering and reduces the close-in fractional spurs at the expense of making the ones far from the carrier larger.

An accumulator is used to keep track of the instantaneous phase error, so that the proper N value can be used and the instantaneous phase error can be compensated for [1]. Although the average N value is correct, the instantaneous value is not correct, and this causes high fractional spurs. In order to deal with the spur levels, a current can be injected into the loop filter to cancel these. The disadvantage of this current compensation technique is that it is difficult to get the correct timing and pulse width for this correction pulse, especially over temperature. Another approach is to introduce a phase delay at the phase detector. This approach yields more stable spurs over temperature, but sometimes adds phase noise. In some parts that use the phase delay compensation technique, it is possible to shut off the compensation circuitry in order to sacrifice reference spur level (typically 15 db) in order to improve the phase noise (typically 5 db). The nature of added phase noise and spurs for fractional parts is very part-specific.

Table 2 shows how a fractional N PLL can be used to generate a 4.3 MHz signal from a 1 MHz comparison frequency, using the phase delay technique. This corresponds to a N value of 4.3. Although N values and frequencies are typically much higher, this example demonstrates how the phase delay and accumulator work without unnecessarily complicating the table. Note that a 4.3 MHz signal has a period of 232.6 nS, and a 1 MHz signal has a period of 1000 nS.

VCO Cycle	Time (nS)	Accumulator (Cycles)	Overflow (Cycles)	Phase Delay (nS)	Compensated Signal to Phase Detector (nS)
4	930.2	0.3	0	69.8	1000
8	1860.5	0.6	0	139.5	2000
12	2970.7	0.9	0	209.3	3000
16	3270.9	0.2	1	279.1	4000
21	4883.7	0.5	0	116.3	5000
25	5814.0	0.8	0	186.0	6000
29	6744.2	0.1	1	255.8	7000
34	7907.0	0.4	0	93.0	8000
38	8837.2	0.7	0	162.8	9000
42	9767.4	0.0	1	232.6	1000
43		This VCO Cycle is swallowed.			

Table 2 *Fractional N Phase Delay Compensation Example*

In Table 2, only the VCO cycles that produce a signal out of the N counter are accounted for. Note that the phase delay is calculated as follows:

$$Phase\ Delay = \frac{1}{VCO\ Frequency} \bullet (Accumulator\ Value + Overflow\ Value)$$

When the accumulator value exceeds one, then an overflow count of one is produced, the accumulator value is decreased by one, and the next VCO cycle is swallowed [1]. Note that in Table 2, this whole procedure repeats every 43 VCO cycles. If a larger N value was chosen for this example, then the same concepts would apply, but Table 2 would be much longer.

Conclusion

The behavior and benefits of the fractional N PLL have been discussed. Although the same theory applies to a fractional N PLL as an integer PLL, the fractional N compensation circuitry can cause many quirky behaviors that are typically not seen in integer N PLLs. For instance, the National Semiconductor LMX2350 PLL has a dual modulus prescaler that requires ***b>=a+2***, instead of ***b>=a***, which is typical of integer N PLLs. Phase noise and spurs can also be impacted by the choice of prescaler as well as by the Vcc voltage to the part. Fractional N PLLs are not for all applications and each fractional N PLL has its own tricks to usage.

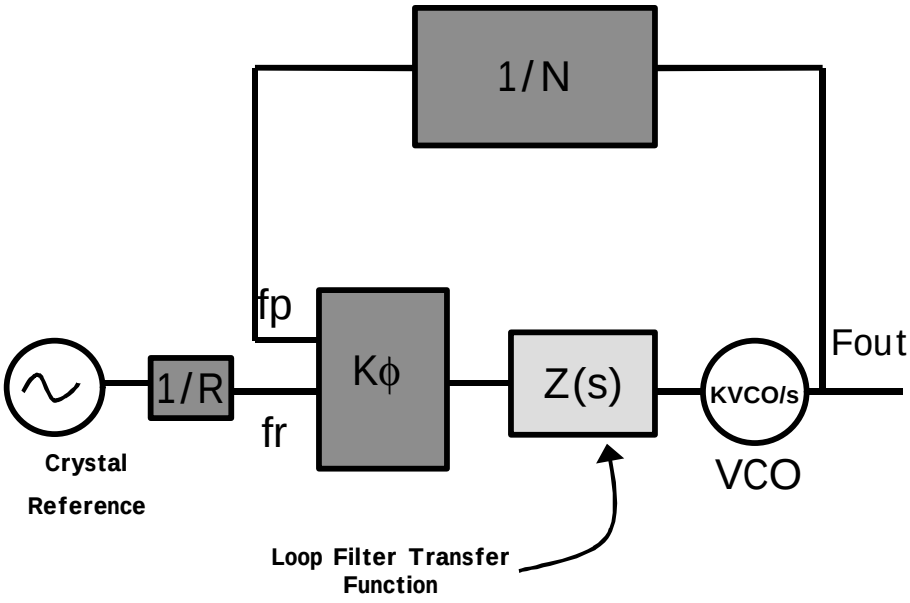
Reference

[1] Best, Roland E., *Phase Locked Loop Theory, Design, and Applications,* 3rd ed, McGraw-Hill, 1995

21. Other PLL Design and Performance Issues

Introduction

This is a collection of small topics that have not been addressed in other chapters. Included topics are N counter determination, the relationship between phase margin and peaking, and counter sensitivity.



N Counter Determination

N Value Determination for a Fixed Output Frequency PLL

In the case that the output frequency of the PLL is to be fixed, the choice of a comparison frequency may not be so obvious. The comparison frequency should always be chosen as large as possible. Recall the relationship between comparison frequency and output frequency:

$$Fout = \left(\frac{N}{R}\right) \bullet Xtal$$

It therefore follows that:

$$\frac{N}{R} = \frac{Fout}{Xtal}$$

Since the output frequency and crystal frequency are both known quantities, the right hand side of this equation is known and can be reduced to a lowest terms fraction. Once this lowest terms fraction is known, the numerator is the N value and the denominator is the R value. If this solution results in illegal N divider ratios, or comparison frequencies that are higher than the phase detector can operate at, then double the N and R values. If there are still problems, then triple them. Keep increasing these quantities until there are no illegal divide ratios and the comparison frequency is within the specification of the part. In the case where there is freedom to choose the crystal frequency, it is best to choose it so that it has a lot of common factors with the output frequency so that the N value is as small as possible.

Variation of Loop Bandwidth with N counter Value, VCO Gain, and Charge Pump Gain

Note that there is a factor of ***1/s*** multiplying the VCO gain, which converts the VCO output from voltage to phase. This gets multiplied by an additional factor of ***1/s*** from transfer function of the loop filter. There are also poles and zeros in this transfer function. The poles should be much greater than the loop bandwidth, and therefore really do not have a large contribution at the frequency equal to the loop bandwidth. There is also a zero in the transfer function and this zero does have some contribution near the loop bandwidth, but this contribution usually small relative to the $1/s^2$ term that comes from taking the ***1/s*** from the transfer function and multiplying this by the ***1/s*** from the VCO gain. From this, it can be concluded that the loop bandwidth is roughly inversely proportional to the square root of the N value. It also follows that the loop bandwidth is roughly proportional square root of the VCO gain and also proportional to the square root of the charge pump gain. It may seem at first that disregarding the poles and zeros of the filter seems like a bold assumption, but simulation and actual testing show that it is not that rough of an assumption. To summarize these results:

$$\frac{wc2}{wc1} = \sqrt{\frac{Kf2}{Kf1}} \bullet \sqrt{\frac{Kvco2}{Kvco1}} \bullet \sqrt{\frac{N1}{N2}}$$

N Value to Design for When the Output Frequency is a Range

From the above equation, it can be seen that the loop bandwidth is roughly inversely proportional to the square root of the N value, so it therefore follows that designing the N value for the geometric mean of the minimum and maximum values minimizes the variation of the loop bandwidth of the PLL from the value for which it was designed. In summary, design for:

$$N = \sqrt{N\,\mathbf{min} \bullet N\,\mathbf{max}}$$

Phase Margin, Stability, and Peaking

The phase margin is related to the stability of the system and a higher phase margin implies more stability. This can be seen by looking at the roots of the closed loop transfer function and tracking how negative the real parts of these roots are. The specific details on this are beyond the scope of this text. On the spectrum analyzer, if the phase margin is very low, then the loop filter response will show a peaking. This section explains why.

Recall that the closed loop transfer function is of the form:

$$CL(s) = \frac{G(s)}{1 + G(s)/N}$$

Of special interest is at the point where the magnitude of $G(s)/N = 1$. The frequency where this occurs is, by definition, the loop bandwidth. The phase of $G(s)/N$ evaluated at the loop bandwidth is also of interest . If this phase is 180 degrees, then the transfer function would have an infinite value and would be unstable. If the phase was zero degrees, then there would be a minimal amount of peaking and maximum stability. Phase margin is therefore defined as the amount of margin on the phase which would be 180 degrees minus the phase of $G(j \bullet wc)/N$. In practice, loop filters with less than 20 degrees phase margin are likely to show instability problems and filters above 80 degrees phase margin have yield components that unrealistic because they are too large, or are negative.

Second order formulas for lock time calculations imply that the lower phase margins imply a faster lock time, but when all poles and zeros are considered, it turns out that the optimal lock time is for phase margins in the 45 to 50 degree range.

On the Pitfalls of Sensitivity

Sensitivity is a feature of real world PLLs. The N counter will actually miscount if too little or too much power is applied to the high frequency input. The limits on these power levels are referred to as the sensitivity. The PLL sensitivity changes as a function of frequency. At the higher frequencies, the curve degrades because the of process limitations, and at the lower frequencies, the curve can also degrade because of problems with the counters making thresholding decisions (the edge rate of the signal is too slow). At the lower frequencies, this limitation can sometimes be addressed by running a square wave instead of a sine wave into the high frequency input of the PLL. Sensitivity can also change from part to part, over voltage, or over temperature. When the power level of the high frequency input approaches sensitivity limits, this can introduce spurs and degradation in phase noise. When the power level gets even closer to this limit, or exceeds it, then the PLL loses lock.

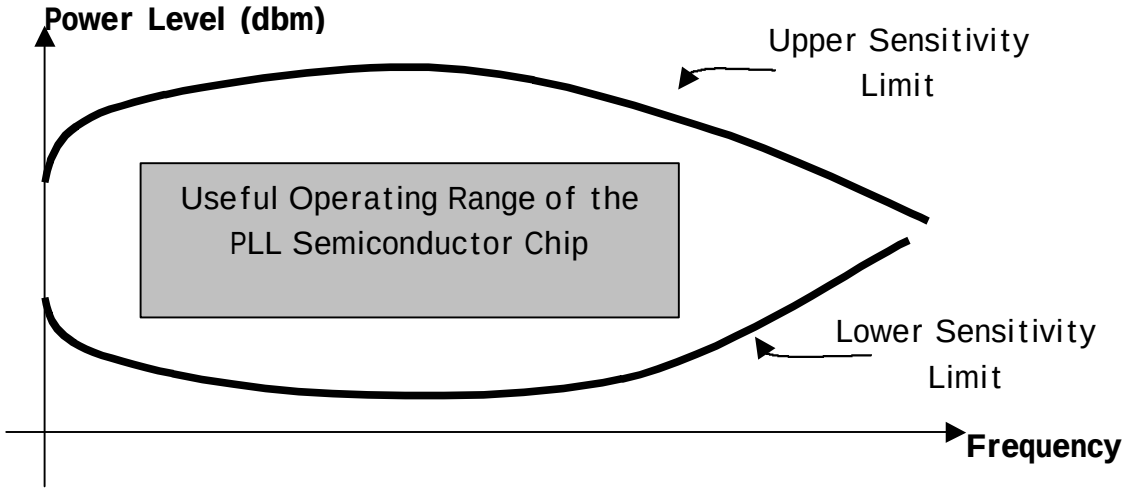


Figure 1 *Typical Sensitivity Curve for a PLL*

The sensitivity curve applies to both the desired signal from the VCO and all of its harmonics. VCO harmonics can especially be troublesome when a part designed for a very high operating frequency is used at a very low operating frequency. Unexpected sensitivity problems can also be agitated by poor matching between the VCO output and the high frequency input of the PLL.

Although sensitivity issues are most common with the N counter, because it usually involves the higher frequency input, these same concepts apply to the R counter as well. In order to for the sensitivity of the PLL to be tested in production, it is necessary to have access to the R and N counters. These test modes are also an excellent way of diagnosing and debugging sensitivity problems. Sensitivity related problems also tend to show a strong dependence on the Vcc voltage and temperature. If poor impedance matching is causing the sensitivity problem, then sometimes pressing one's finger on the part will temporarily make the problem go away. This is because the input impedance of the part is being impacted.

Sensitivity problems with either the N or R can cause spurs to appear, increase phase noise, or cause the PLL to tune to a different frequency than it is programmed to. In more severe cases, they can cause the PLL to steer the VCO to one of the power supply rails. N counter sensitivity problems usually cause the VCO to go higher than it should. R counter sensitivity problems usually cause the PLL to tune lower than it should. In either case, the VCO output is typically very noisy. Figure 2 shows a PLL locking much lower than it is programmed to lock due to an R counter sensitivity problem. It is also possible for the N counter to track a higher harmonic of the VCO signal, which causes the PLL to tune the VCO lower than it should. This problem is most common when parts are operated at frequencies much lower than they are designed to run at. One should be aware that it is possible to be operating within the datasheet specifications for sensitivity with a few dB of margin, and still have degraded phase noise as a result of a sensitivity problem. This is because the datasheet specification for sensitivity is a measurement of when the counters actually miscount, not when they become noisy.

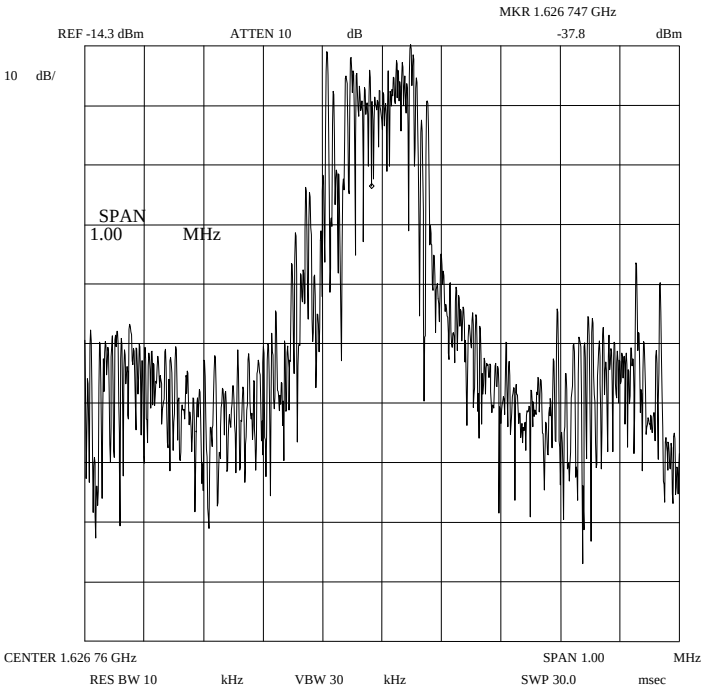


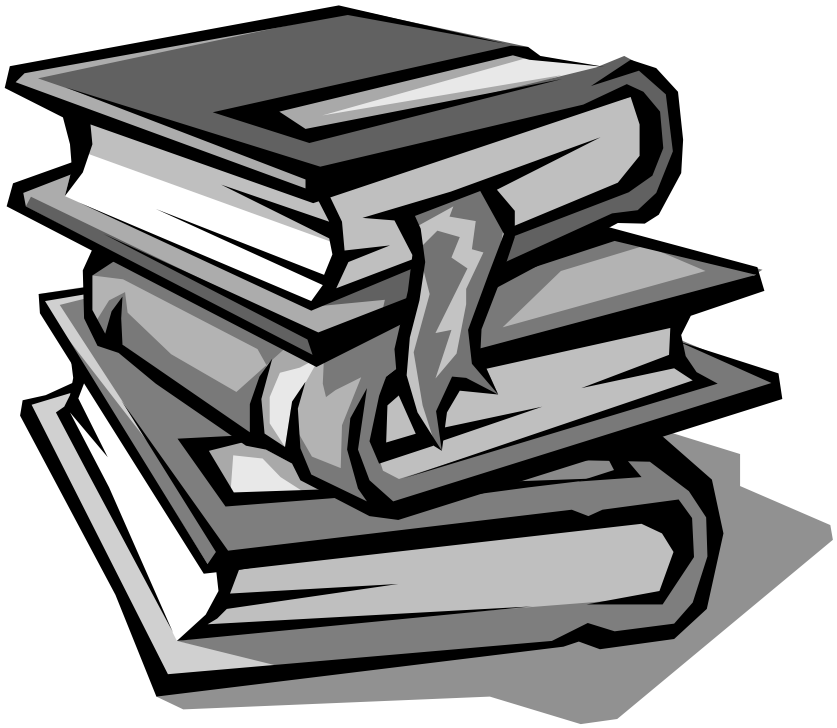
Figure 2 *PLL Locking to Wrong Frequency Due to R Counter Sensitivity Problem*

Conclusion and Author's Parting Remarks

This chapter has addressed some of the issues not addressed in other chapters. The reader who has reached this point in this book should hopefully have an appreciation on how involved PLL design and simulation can be.

It was the aim of this book to tell the reader everything they wanted to know, and things they probably never cared to know about the designing and simulating a PLL frequency synthesizer. However, there are still many other topics that have been left out. The concepts presented in this book have come from a solid theoretical understanding backed with measured data and practical examples. All of the data in this book was gathered from various National Semiconductor Synthesizer chips, which include the R counter, N counter, charge pump, and phase-frequency detector.

Supplemental Information



22. Glossary and Abbreviation List

ATTEN
The attenuation index, which is intended to give an idea of the spurious attenuation added by the components R3 and C3 in the loop filter of other loop filter design papers, but not this book. Also used in reference to the attenuation of a resistive pad in dB.

Channel and Channel Spacing
In many applications, a set of frequencies is to be generated that are evenly spaced apart. These frequencies to be generated are often referred to as channels and the spacing between these channels is often referred to as the channel spacing.

Charge Pump
Used in conjunction with the phase-frequency detector, this device outputs a current of constant amplitude, but variable polarity and duty cycle. It is usually modeled as a device that outputs a steady current of value equal to the time-averaged value of the output current.

Closed Loop Transfer Function , CL(s) (see Figure 3)
This is given by $\frac{G(s)}{1+G(s)\bullet H}$, where $H=\frac{1}{N}$ and G(s) is the Open Loop Transfer Function

Comparison Frequency, Fcomp (see Figure 1)
The crystal reference frequency divided by R. This is also sometimes called the reference frequency.

Continuous Time Approximation
This is where the discrete current pulses of the charge pump are modeled as a continuous current with magnitude equal to the time-averaged value of the current pulses.

Control Voltage , Vtune (see Figure 1)
The voltage that controls the frequency output of a VCO.

Crystal Reference, Xtal (see Figure 1)
A stable and accurate frequency that is used for a reference.

Damping Factor , ζ (see Figure 5)
For a second order transient response, this determines the shape of the exponential envelope that multiplies the frequency ringing.

Dead Zone
This is a property of the phase frequency detector caused by component delays. Since the components making up the PFD have a non-zero delay time, this causes the phase detector to be insensitive to very small phase errors.

Dead Zone Elimination Circuitry
This circuitry can be added to the phase detector to avoid having it operating in the dead zone. This usually works by causing the charge pump to always come on for some minimum amount of time.

Fractional Modulus
The fractional denominator used for in the fractional word.

Fractional N PLL
A PLL in which the N divider value can be a fraction.

Fractional Spur
Spurs that occur in a fractional N PLL at multiples of the comparison frequency divided by the fractional modulus that are caused by the PLL.

Frequency Jump, Fj (see Figure 5)
When discussing the transient response of the PLL, this refers to the frequency difference between the frequency the PLL is initially at, and the final target frequency.

Frequency Synthesizer
This is a PLL that has a high frequency divider (N divider), which can be used to synthesize a wide variety of signals.

Frequency Tolerance
In regards to calculating or measuring lock time, this is the frequency error that is acceptable. If the frequency error is less than the frequency tolerance, the PLL is said to be in lock. Typical values for this are 500 Hz or 1 KHz.

G(s)
This represents the loop filter impedance multiplied by the VCO gain and charge pump gain, divided by s.

$$G(s) = \frac{Kf \bullet Kvco}{s} \bullet Z(s)$$

Kvco
The gain of the VCO expressed in MHz/V.

Kϕ
This is the gain of the charge pump expressed in mA/(2π radians)

Locked PLL
A PLL such that the output frequency divided by N is equal to the comparison frequency within acceptable tolerances.

Lock Time **(see Figure 5)**
The time it takes for a PLL to switch from an initial frequency to a final frequency for a given frequency jump to within a given tolerance.

Loop Bandwidth , ωc **(see Figures 2,3, and 4)**
The frequency at which the magnitude of the open loop transfer function is equal to 1. ωc is intended to be the true loop bandwidth, while ωp is an mathematical approximation to ωc.

Loop Filter
A low pass filter that takes the output currents of the charge pump and turns them into a voltage, used as the tuning voltage for the VCO. Z(s) is often used to represent the impedance of this function. Although not perfectly accurate, some like to view the loop filter as an integrator.

Modulation Domain Analyzer **(see Figure 5)**
A piece of RF equipment that displays the frequency vs. time of an input signal.

Modulation Index , β
This is in reference to a sinusoidally modulated RF signal. The formula is given below, where F(t) stands for the frequency of the signal.

$$F(t) = const. + F_{dev} \bullet \cos(w_m \bullet t)$$

$$b = \frac{F_{dev}}{w_m}$$

Natural Frequency , ωn **(see Figure 5)**
For a second order transient response, this is the frequency of the ringing of the frequency response.

Open Loop Transfer Function , G(s) **(see Figure 2)**
The transfer function which is obtained by taking the product of the VCO Gain, Charge Pump Gain (This includes the Phase Detector Gain) and Loop Filter Impedance divided by N.

$$G(s) = \frac{Kf \bullet Kvco \bullet Z(s)}{N \bullet s}$$

Overshoot **(see Figure 5)**
For the second order transient response, this is the amount that the target frequency is initially exceeded before it finally settles in to the proper frequency

Phase Detector **(see Figure 1)**
A device that produces an output signal that is proportional to the phase difference of its two inputs.

Phase-Frequency Detector **(see Figure 1)**
Very similar to a phase detector, but it also produces an output signal that is proportional to the frequency error as well.

Phased Locked Loop, PLL **(see Figure 1)**
A circuit that uses feedback control to produce an output frequency from a fixed crystal reference frequency. Note that a PLL does not necessarily have an N divider. In the case that it does, it is referred to as a frequency synthesizer, which is the subject of this book.

Phase Margin, ϕ
180 degrees minus phase of the open loop transfer function at the loop bandwidth. Loop filters are typically designed for a phase margin between 30 and 70 degrees. Simulations show that around 48 degrees yields the fastest lock time. The formula is given below:

$$f = 180 - \angle C(j \bullet wc)$$

Phase Noise **(see Figure 4)**
This is noise on the output phase of the PLL. Since phase and frequency are related, it is visible on a spectrum analyzer. Within the loop bandwidth, the PLL is the dominant noise source. The metric used is dBc/Hz (decibel relative to the carrier per Hz). This is typically normalized to a 1 Hz bandwidth by subtracting 10*(Resolution Bandwidth) of the spectrum analyzer.

Phase Noise Floor
This is the phase noise minus ***20•log(N).*** Note that this is generally not a constant because it tends to be dominated by the charge pump, which gets noisier at higher comparison frequencies.

Prescaler
Frequency dividers included as part of the N divider used to divide the high frequency VCO signal down to a lower frequency.

N Divider **(see Figure 1)**
A divider that divides the high frequency (and phase) output by a factor of N.

R Divider **(see Figure 1)**
A divider that divides the crystal reference frequency (and phase) by a factor of R.

Reference Spurs
Undesired frequency spikes on the output of the PLL caused by leakage currents and mismatch of the charge pump that FM modulate the VCO tuning voltage.

Resolution Bandwidth , RBW
See definition for Spectrum Analyzer.

Sensitivity
Power limitations to the high frequency input of the PLL chip (from the VCO). At these limits, the counters start miscounting the frequency and do not divide correctly.

Smith Chart
A chart that shows how the impedance of a device varies over frequency.

Spectrum Analyzer, SA **(see Figure 4)**
A piece of RF equipment that displays the power vs. frequency for an input signal. This piece of equipment works by taking a frequency ramp function and mixing it with the input frequency signal. The output of the mixer is filtered with a bandpass filter, which has a bandwidth equal to the resolution bandwidth. The narrower the bandwidth of this filter, the less noise that is let through.

Spurious Attenuation **(see Figure 3)**
This refers to the degree to which the loop filter attenuates the reference spurs. This can be seen in the closed loop transfer function.

Spur Gain, SG
This refers to the magnitude of the open loop transfer function evaluated at the comparison frequency. This gives a good indication of how the reference spurs of two loop filters compare.

T31 Ratio
This is the ratio of the poles of a third order loop filter. If this ratio is 0, then this is actually a second order filter. If this ratio is 1, then this turns out to be the value for this parameter that yields the lowest reference spurs.

Temperature Compensated Crystal Oscillator, TCXO
A crystal that is temperature compensated for improved frequency accuracy

Tolerance, tol **(see Figure 5)**
The acceptable frequency error to within which the PLL is considered locked.

Varactor Diode
This is a diode inside a VCO that is reverse biased. As the tuning voltage to the VCO changes, it varies the junction capacitance of this diode, which in turn varies the VCO voltage.

Voltage Controlled Oscillator, VCO **(see Figure 1)**
A device that produces an output frequency that is dependent on an input (Control) voltage.

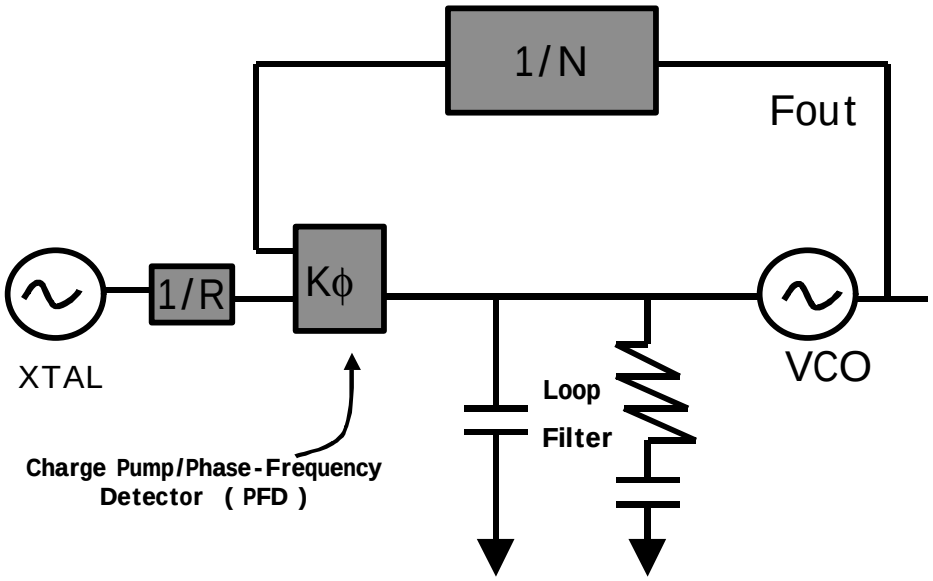


Figure 1 *Basic PLL (Frequency Synthesizer) Diagram*

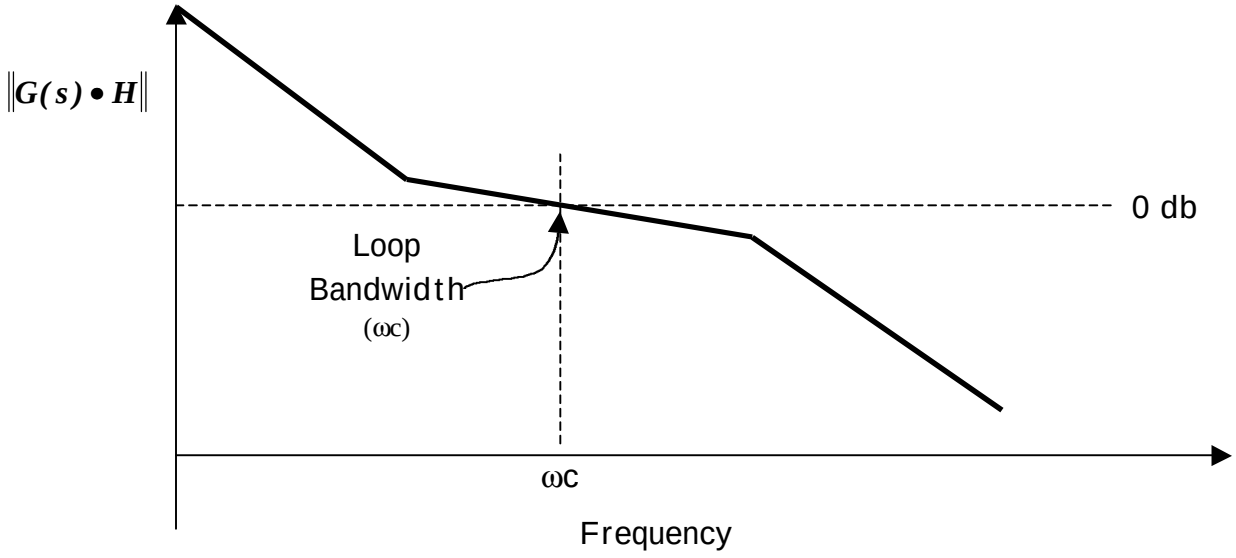


Figure 2 *Open Loop Response of a PLL*

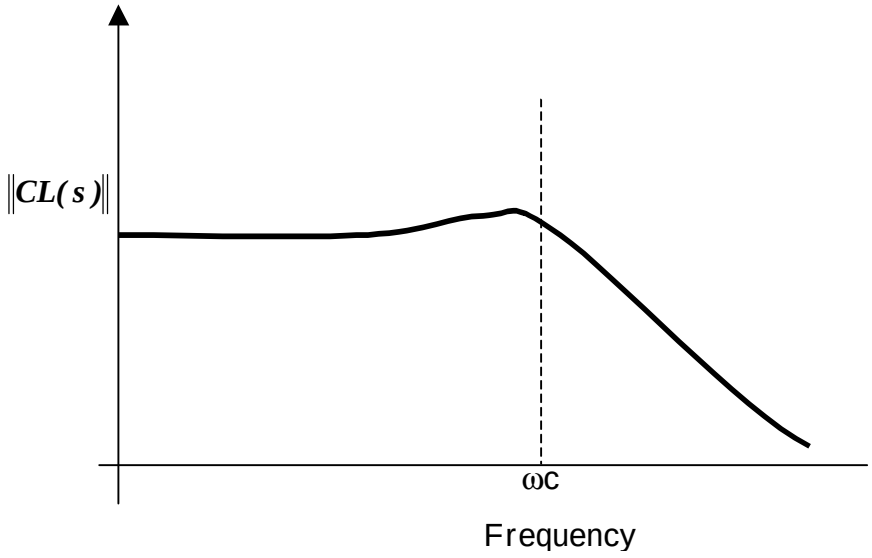


Figure 3 *Typical Closed Loop Transfer Function for a PLL*

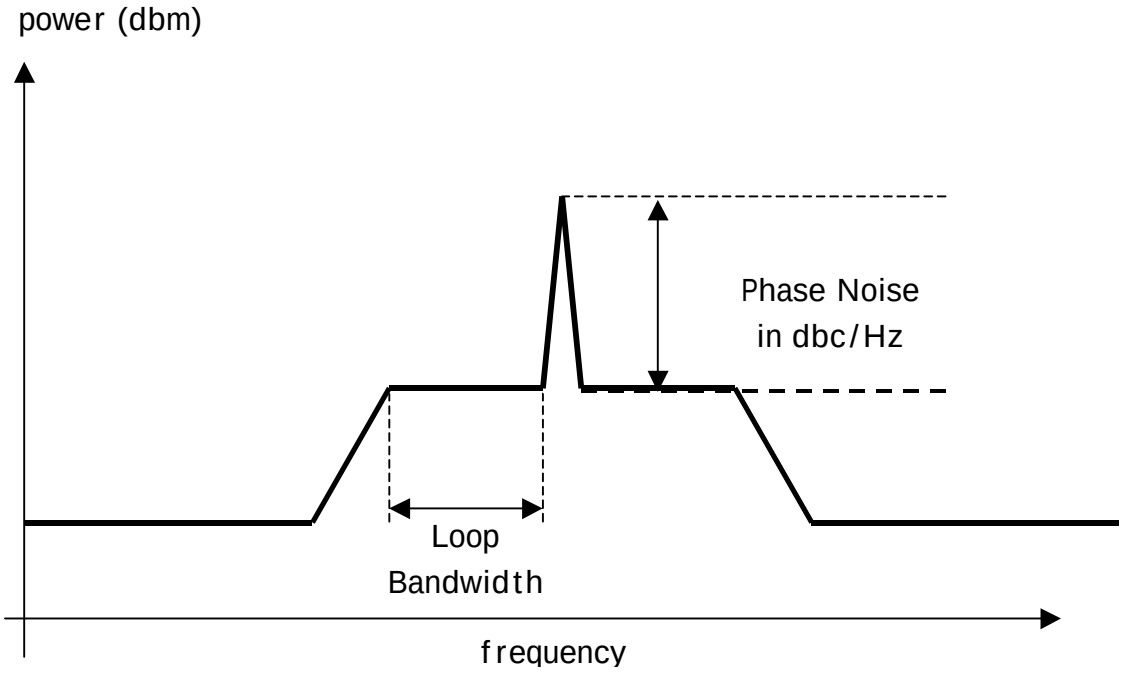


Figure 4 *Typical Phase Noise Spectral Plot for a PLL*

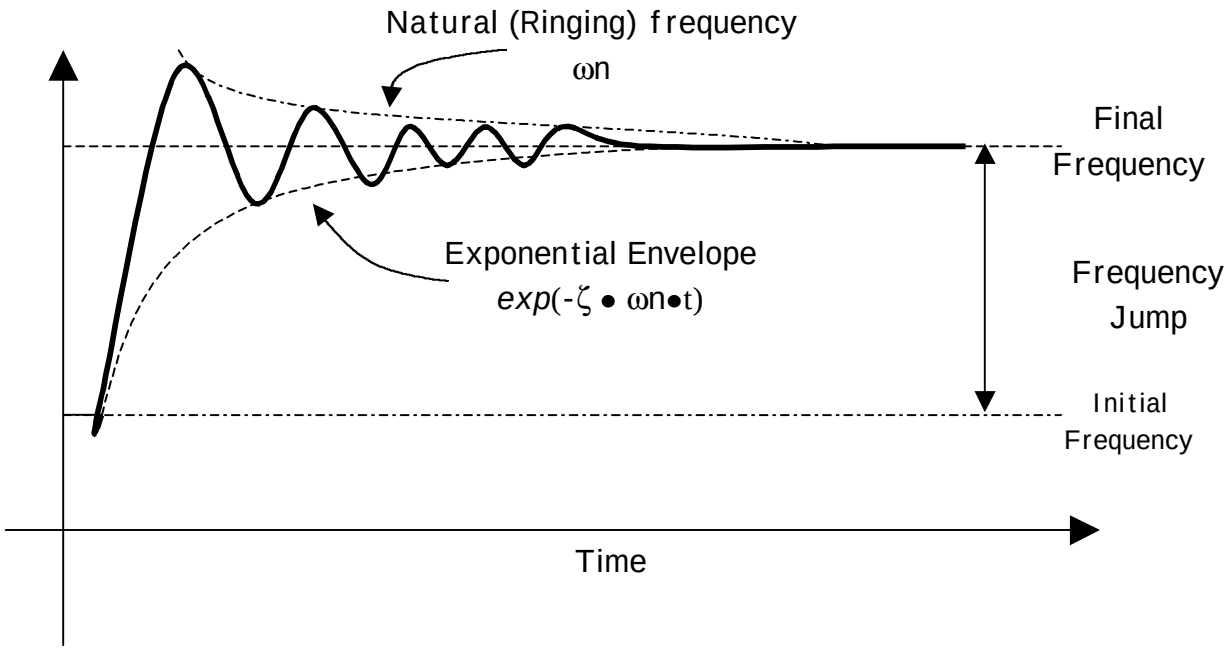


Figure 5 *Typical Transient Response of a PLL*

Abbreviation List

Loop Filter Parameters

C1, C2, C3, and C4	Loop filter capacitor values
CL(s)	Closed loop PLL transfer function
f	Frequency of interest in Hz
Fc	Loop bandwidth in KHz
Fcomp	Comparison frequency
Fj	Frequency jump for lock time
Fout	VCO output frequency
Fp	VCO frequency divided by N
Fr	XTAL frequency divided by R
Fspur	Spur Frequency
G(s)	Loop filter transfer function
H	PLL feedback, which is 1/N
i, j	The complex number $\sqrt{-1}$
Kϕ	Charge pump gain in mA/(2π radians)
Kvco	VCO gain in MHz/V
N	The N counter Value
PLL	Phased Locked Loop
R	The R counter Value
R2, R3, and R4	Loop filter resistor values
s	Laplace transform variable = 2π•f•j
T2	The zero in the loop filter transfer function
T1, T3, T4	The poles in the loop filter transfer function
T31	The ratio of the pole T3 to the pole T1
T41	The ratio of the pole T4 to the pole T1
tol	Frequency tolerance for lock time
Vcc	The main power supply voltage
Vdo	The output voltage of the PLL charge pump
VCO	Voltage Controlled Oscillator
Vpp	The power supply voltage for the PLL charge pump
XTAL	Crystal Reference or Crystal Reference Frequency
Z(s)	Loop filter impedance

Greek Symbols

β	The modulation index
ϕ	The phase margin
ϕr	The XTAL phase divided by R
ϕp	The VCO phase divided by N
ω	The frequency of interest in radians
ωc	The loop bandwidth in radians
ωn	Natural Frequency
ζ	Damping Factor

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24. Useful Websites and Online RF Tools

http://www.anadigics.com/engineers/Receiver.html

Online receiver chain analysis tool for calculation of gain, noise figure, third order intercept point, and more.

http://www.emclab.umr.edu/pcbtlc/microstrip.html

This is an online microstrip impedance calculator that is useful in calculating the impedance of a PCB trace. It is very easy to use and also can be used to calculate the desired trace width in order to produce a desired impedance

http://www.geocities.com/szu_lan/

The author's personal website with both personal and professional information.

http://home.rodchester.rr.com/lascari/lancepll.zip

Lance Lascari's Mathcad PLL Analysis Software. This does require mathcad to run, but has some excellent phase noise analysis tools in it.

http://www.rfcafe.com

RF Café has an online discussions, definitions, and RF Tools.

http://rf.rfglobalnet.com/software_modeling/home.htm

RF Globalnet has an online discussion forum and also has a lot of free RF simulation tools that can be downloaded.

http://www-sci.lib.uci.edu/HSG/RefCalculators.html

Jim Martindale's calculators for everything you can think of.

http://www.treasure-troves.com

The "Rolls Royce" of mathematics online reference site on the web. There is also a corresponding book, which is excellent. Compiled by Eric Weisstein.

http://wireless.national.com

National Semiconductor's wireless portal site with EasyPLL program largely based on this book. There is also a lot of other useful information and RF tools there too.