An Analysis and Performance Evaluation of a Passive Filter Design Technique for Charge Pump Phase-Locked Loops

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The high performance of today's digital phase-lock loop makes it the preferred choice for generation of stable, low noise, tunable local oscillators in wireless communications applications. This paper investigates the design of passive loop filters for Frequency Synthesizers utilizing a Phase-Frequency Detector and a current switch charge pump such as National Semiconductor's PLLatinum™ Series. Passive filter design for a TYPE II third order phase-lock loop is discussed in depth, with some discussion of higher order filters included. Specific test results are presented for a GSM synthesizer design. Optimization of phase-lock loop performance with respect to different parameters is discussed.

The basic phase-lock-loop configuration we will be considering is shown in *Figure 1*. The PLL consists of a high-stability crystal reference oscillator, a frequency synthesizer such as the National Semiconductor LMX2315TM, a voltage controlled oscillator (VCO), and a passive loop filter. The frequency synthesizer includes a phase detector, current mode charge pump, and programmable frequency dividers. A passive filter is desirable for its simplicity, low cost, and low phase noise.

In most standard PLL's there are several design parameters which can be treated as constant values. This linear approximation provides a good estimation of loop performance. The values of the PLL filter design constants depend on the specific application. For example, Kϕ is determined by the synthesizer charge pump output current magnitude. The notation and definitions for these values along with standard units used throughout this paper are given in Table I below.

TABLE I. PLL Filter Design Constants

Kvco - (MHz/Volt)

Voltage Controlled Oscillator (VCO) Tuning Voltage constant. The frequency vs voltage tuning ratio.

Kϕ - (mA/2πrad)

Phase detector/charge pump constant. The ratio of the current output to the input phase differential.

RFopt - (MHz)

Radio Frequency output of the VCO at which the loop filter is optimized.

Fref - (kHz)

Frequency of the phase detector inputs. Usually equivalent to the RF channel spacing.

N

Main divider ratio. Equal to RFopt/Fref.

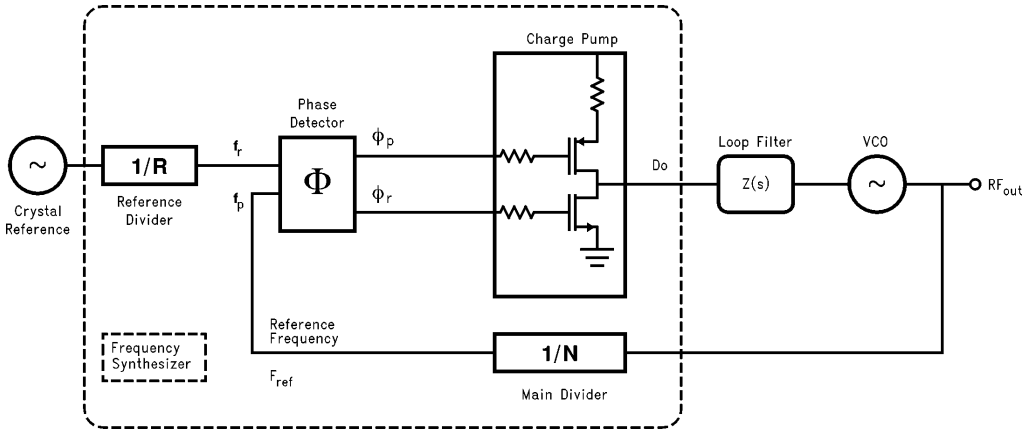

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FIGURE 1. Basic Charge Pump Phase Locked Loop

Some basic knowledge of control loop theory is necessary in order to understand PLL filter dynamics. For a more thorough treatment consult references [1] through [6]. A linear mathematical model representing the phase of the PLL in the locked state is presented in *Figure 2*. An additional integrator is needed in the transfer function for the forward gain and is usually lumped together with the VCO in the literature, references [1-4]. Using the simplified diagram in *Figure 2*, and feedback theory, one may obtain the equations for the phase transfer functions presented in Table II.

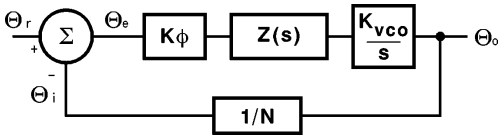

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FIGURE 2. PLL Linear Model

TABLE II. PLL Phase Transfer Functions

Forward loop gain = G(s) = Θo/Θe = **Kϕ Z(s) Kvco/s**
Reverse loop gain = H(s) = Θi/Θo = **1/N**
Open loop gain = H(s) G(s) = Θi/Θe = **Kϕ Z(s)Kvco/Ns**
Closed loop gain = Θo/Θr = **G(s)/ [1 + H(s) G(s)]**

The standard passive loop filter configuration for a type II current mode charge pump PLL is shown in *Figure 3*. The loop filter is a complex impedance in parallel with the input capacitance of the VCO, or in other words, a driving point immitance.

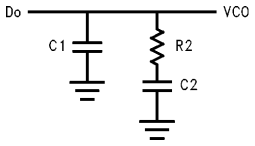

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FIGURE 3. 2nd Order Passive Filter

The phase detector's current source outputs pump charge into the loop filter, which then converts the charge into the VCO's control voltage. The shunt capacitor C1 is recommended to avoid discrete voltage steps at the control port of the VCO due to the instantaneous changes in the charge pump current output. A low pass filter section may be needed for some high performance synthesizer applications that require additional rejection of the reference sidebands, known as spurs.

One method of filter design uses the open loop gain bandwidth and phase margin to determine the component values. Locating the point of minimum phase shift at the unity gain frequency of the open loop response as shown in *Figure 4* ensures loop stability. The phase relationship between the pole and zero also allows easy determination of the loop filter component values. The phase margin, ϕ_p, is defined as the difference between 180° and the phase of the open loop transfer function at the frequency, ω_p, corresponding to 0-dB gain. The phase margin is chosen between 30° and 70°. When designing for a higher phase margin you trade off higher stability for a slower loop response time and less attenuation of Fref. A common rule of thumb is to begin your design with a 45° phase margin.

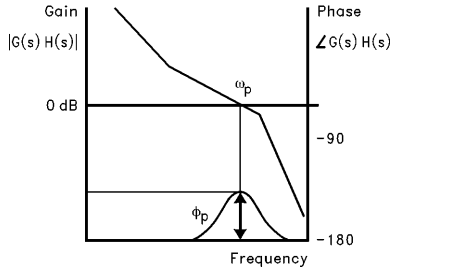

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FIGURE 4. Open Loop Response Bode Plot

The impedance of the second order filter in *Figure 3* is

$$Z(s) = \frac{s(C2 \bullet R2) + 1}{s^2 (C1 \bullet C2 \bullet R2) + sC1 + sC2} \quad (1)$$

Define the time constants which determine the pole and zero frequencies of the filter transfer function by letting

$$T1 = R2 \bullet \frac{C1 \bullet C2}{C1 + C2} \quad (2a) \qquad T2 = R2 \bullet C2 \quad (2b)$$

Thus the 3rd order PLL Open Loop Gain in Table II can be calculated in terms of frequency, ω, the filter time constants T1 and T2, and the design constants Kϕ, Kvco, and N.

$$G(s) \bullet H(s)\Big|_{s=j\bullet\omega} = \frac{-Kpd \bullet Kvco\,(1 + j\omega \bullet T2)}{\omega^2\, C1 \bullet N\,(1 + j\omega \bullet T1)} \bullet \frac{T1}{T2} \quad (3)$$

From equation 3 we can see that the phase term will be dependent on the single pole and zero such that the phase margin is determined in equation 4. The available phase margin therefore is proportional to the ratio of C1 and C2.

$$\phi(\omega) = \tan^{-1}(\omega \bullet T2) - \tan^{-1}(\omega \bullet T1) + 180° \quad (4)$$

By setting the derivative of the phase margin equal to zero as shown in equation 5,

$$\frac{d\phi}{d\omega} = \frac{T2}{1 + (\omega \bullet T2)^2} - \frac{T1}{1 + (\omega \bullet T1)^2} = 0 \quad (5)$$

the frequency point corresponding to the phase inflection point is found in terms of the filter time constants T1 and T2. This relationship is given in equation 6.

$$\omega_p = 1/\sqrt{T2 \bullet T1} \quad (6)$$

To insure loop stability, we want the phase margin to be maximum when the magnitude of the open loop gain equals 1. Equation 3 then gives

$$C1 = \frac{Kpd \bullet Kvco \bullet T1}{\omega_p{}^2 \bullet N \bullet T2} \left\| \frac{(1 + j\omega_p \bullet T2)}{(1 + j\omega_p \bullet T1)} \right\| \quad (7)$$

Therefore, if the loop bandwidth, ω_p, and the phase margin, ϕ_p, are specified, equations 1 through 7 allow us to calculate the two time constants, T1 and T2.

The formulas for T1 and T2 are shown in equations 8 and 9.

$$T1 = \frac{\sec \phi_p - \tan \phi_p}{\omega_p} \quad (8)$$

$$T2 = \frac{1}{\omega_p{}^2 \bullet T1} \quad (9)$$

From the time constants, T1, T2, and the loop bandwidth, ω_p, the values for C1, R2, and C2 are obtained in equations 10 to 12.

$$C1 = \frac{T1}{T2} \bullet \frac{Kpd \bullet Kvco}{\omega_p{}^2 \bullet N} \sqrt{\frac{1 + (\omega_p \bullet T2)^2}{1 + (\omega_p \bullet T1)^2}} \quad (10)$$

$$C2 = C1 \bullet \left(\frac{T2}{T1} - 1 \right) \quad (11)$$

$$R2 = \frac{T2}{C2} \quad (12)$$

Current switching noise in the dividers and the charge pump at the reference rate, Fref, may cause unwanted FM sidebands at the RF output. In wireless communications, the phase detector comparison frequency is generally a multiple of the RF channel spacing. These spurious sidebands can cause noise in adjacent channels. Additional filtering of the reference spurs is often times necessary, depending on how narrow your loop filter is. This is usually the case in today's TDMA digital cellular standards, such as GSM, PDC, PHS, or IS-54. The sub-millisecond lock times necessary for switching between channel frequencies makes a relatively wide loop filter mandatory. For these performance critical synthesizer applications placing a series resistor and a shunt capacitor prior to the VCO provides a low pass pole for more attenuation of unwanted spurs. The use of a passive loop filter eliminates the noise contributions from an op amp in an active filter. This is critical due to the strict RMS. phase error, and integrated phase noise requirements. The recommended filter configuration is shown in *Figure 5*.

The added attenuation from the low pass filter is:

$$ATTEN = 20 \log [(2\pi Fref \bullet R3 \bullet C3)^2 + 1] \quad (13)$$

Defining the additional filter time constant as

$$T3 = R3 \bullet C3 \quad (14)$$

Then in terms of the attenuation of the reference spurs added by the low pass pole we have

$$T3 = \sqrt{\frac{10^{(ATTN/20)} - 1}{(2\pi \bullet Fref)^2}} \quad (15)$$

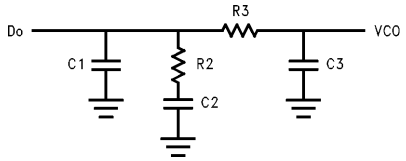

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FIGURE 5. 3rd Order Lowpass Filter

The additional pole must be lower than the reference frequency, in order to significantly attenuate the spurs, but must be at least 5 times higher than the loop bandwidth, or the loop will almost assuredly become unstable. In order to compensate for the added low pass section, the filter component values are recalculated using the new open loop unity gain frequency, ω_c, as in equation 17. The degradation of phase margin caused by the added low pass is then mitigated by slightly increasing C1 and C2 while slightly decreasing R2. Note that ω_c is slightly $< \omega_p$, therefore the frequency jump lock time will increase. Although not exact, the linear assumptions used in this design technique provide suprisingly good results for loop filter bandwidths of up to 1/5 of the reference rate. The derivation of ω_c is included in the appendix.

$$T2 = 1/[\omega_c{}^2 \bullet (T1 + T3)] \quad (16)$$

$$\omega_c = \frac{\tan \phi \bullet (T1 + T3)}{[(T1 + T3)^2 + T1 \bullet T3]} \times \left[\sqrt{1 + \frac{(T1 + T3)^2 + T1 \bullet T3}{[\tan \phi \bullet (T1 + T3)]^2}} - 1 \right] \quad (17)$$

$$C1 = \frac{T1}{T2} \frac{Kpd \bullet Kvco}{\omega_c{}^2 \bullet N} \times \left[\frac{(1 + \omega_c{}^2 \bullet T2^2)}{(1 + \omega_c{}^2 \bullet T1^2)(1 + \omega_c{}^2 \bullet T3^2)} \right]^{1/2} \quad (18)$$

Similar to the 2nd Order filter we have

$$C2 = C1 \bullet \left(\frac{T2}{T1} - 1 \right); \quad (11)$$

$$R2 = \frac{T2}{C2} \quad (12)$$

The only component values that need to be determined comprise the added low pass pole. Since these values are solely determined from equations 13 and 14, their values are somewhat arbitrary. It is not prudent, however to have a capacitor value for C3 which is equal to or greater than the other capacitors. As rule of thumb choose C3 $\leq$ C1/10, otherwise T3 will interact with the primary poles of the filter. Likewise, choose R3 at least twice the value of R2. When selecting C3 you must also take into account the input capacitance of the VCO tuning varactor diode which will add in parallel.

The following example is a typical synthesizer developed for the Global System Mobile (GSM) digital cellular standard using the described filter design technique. The RF channel spacing is 200 kHz, and a typical synthesizer frequency range is from 865 MHz–915 MHz. Since the addition of a low pass filter will reduce the closed loop bandwidth slightly, select an initial design value which is slightly larger than desired.

Example

$$\mathbf{Kvco} = 20\ \text{MHz/V}.$$

$$\mathbf{Kphi} = 5\ \text{mA}$$

$$\mathbf{RFopt} = 900\ \text{MHz}$$

$$\mathbf{Fref} = 200\ \text{kHz}$$

$$\mathbf{N} = \mathbf{RFopt/Fref} = 4500$$

$$\omega_{\mathbf{p}} = 2\pi * 20\ \text{kHz} = 1.256e5$$

$$\phi_{\mathbf{p}} = 45°$$

$$\mathbf{ATTEN} = 20\ \text{dB}$$

$$T1 = \frac{\sec \phi_p - \tan \phi_p}{\omega_p} = 3.29e-6$$

$$T3 = \sqrt{\frac{10^{(20/20)} - 1}{(2\pi \bullet 200e3)^2}} = 2.387e-6$$

$$\omega_c = \frac{(3.29e-6 + 2.387e-6)}{[(3.29e-6 + 2.387e-6)^2 + 3.29e-6 \bullet 2.387e-6]} \times \left[\sqrt{1 + \frac{(3.29e-6 + 2.387e-6)^2 + 3.29e-6 \bullet 2.387e-6}{[(3.29e-6 + 2.387e-6)]^2}} - 1\right]$$

$$\omega_c = 7.045e4$$

$$T2 = \frac{1}{(7.045e4)^2 \bullet (3.29e-6 + 2.387e-6)} = 3.549e-5$$

$$C1 = \frac{3.29e-6}{3.549e-5} \frac{(5.0e-3) \bullet 20e+6}{(7.045e4)^2 \bullet 4500} \times \left[\frac{[1 + (7.045e4)^2 \bullet (3.549e-5)^2]}{[1 + (7.045e4)^2 \bullet (3.29e-6)^2 \parallel 1 + (7.045e)^2 \bullet (2.39e-6)^2]}\right]^{1/2}$$

$$C1 = 1.085\ \text{nF}$$

$$C2 = 1.085\ \text{nF} \bullet \left(\frac{3.55e-5}{3.29e-6} - 1\right) = 10.6\ \text{nF};$$

$$R2 = \frac{3.55e-5}{10.6e-9} = 3.35\ \text{k}\Omega;$$

if we choose $R3 = 22\ \text{k}\Omega$;

then $$C3 = \frac{2.34e-6}{22e3} = 106\ \text{pF}$$

Converting the calculated numbers to standard component values gives the filter shown in the test board schematic for the synthesizer implementation, *Figure 6*.

Test results for the PLL loop filter design using a National Semiconductor LMX2315 Frequency Synthesizer are shown in the following pages. A 10 MHz crystal oscillator was used as the reference oscillator input signal. The supply voltage was 5V, and the entire current consumption, including the VCO, was <15 mA.

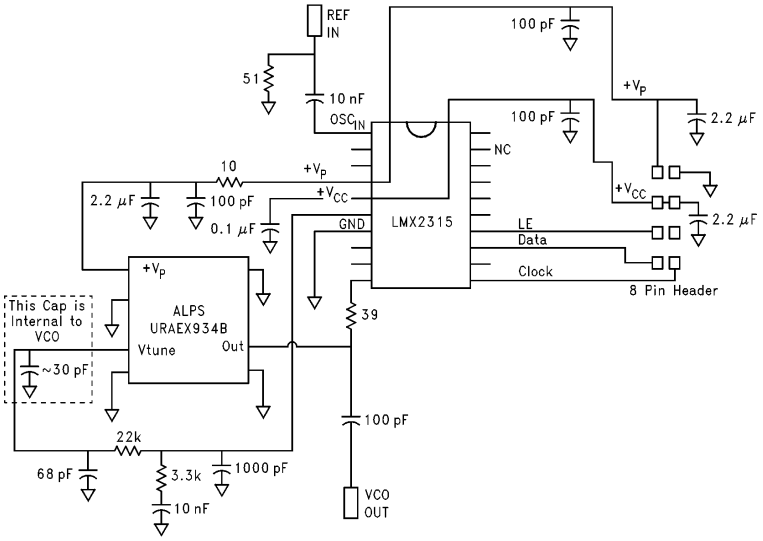

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FIGURE 6. Test Fixture Schematic

Figures 7 to *9* show HP8566 Spectrum Analyzer measurements of the RF output. The measured closed loop filter bandwidth is between 15 kHz and 17.5 kHz. The reference spurious level is ≤70 dBc, due to the loop filter attenuation and the low spurious noise level of the LMX2315. The phase noise level at 1 kHz offset in *Figure 9* is −79.5 dBc/Hz. This correlates to a phase noise floor of ≤150 dBc/Hz. The relatively flat PLL closed loop characteristics gives a measured RMS. phase error of <2°, and is also an indicator of good loop stability.

Of concern in any PLL loop filter design is the time it takes to lock in to a new frequency when switching channels. The HP53310A Modulation Domain Analyzer plots in *Figures 10* and *11* show the positive and negative switching waveforms for a frequency jump of 865 MHz–915 MHz. The well balanced charge pump of the LMX2315 frequency synthesizer causes the waveforms to be nearly inverted replicas of each other. Narrowing the frequency span of the HP53310A Modulation Domain Analyzer enables evaluation of the frequency lock time to within ±500 Hz. The lock time is seen in *Figure 12* to be <500 μs for a frequency jump of 50 MHz.

CONCLUSION

An analysis of a frequency domain design technique for passive filters in charge pump phase-locked loops was presented. Measurements of a PLL designed using this method show good results in a practical synthesizer realization. The results demonstrate a high performance synthesizer in conjunction with a passive loop filter provide a fast switching, low noise frequency source for today's challenging digital wireless telecommunications standards.

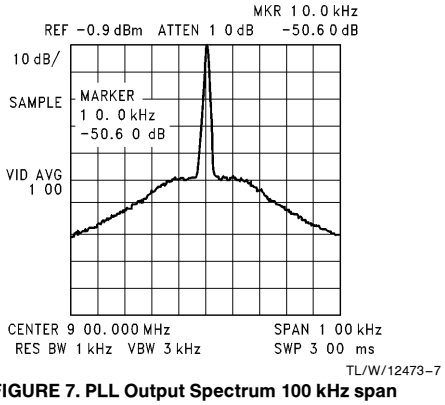

FIGURE 7. PLL Output Spectrum 100 kHz span

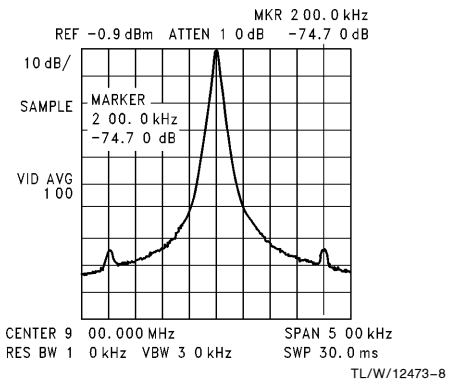

FIGURE 8. PLL 200 kHz Reference spurs

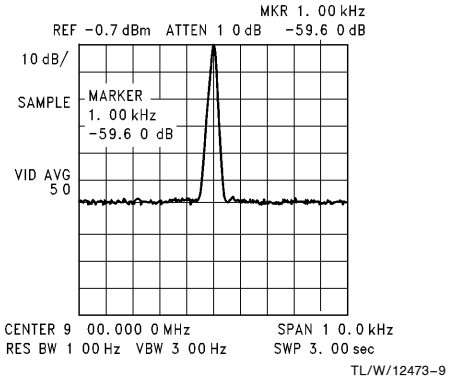

FIGURE 9. PLL Close in Phase Noise

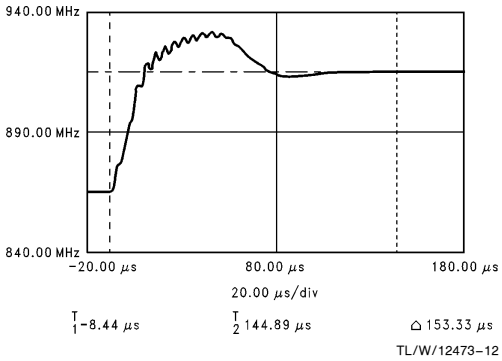

FIGURE 10. PLL Positive Frequency Jump Waveform

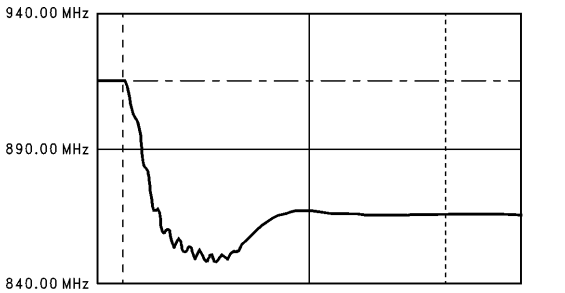

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FIGURE 11. PLL Negative Frequency Jump Waveform

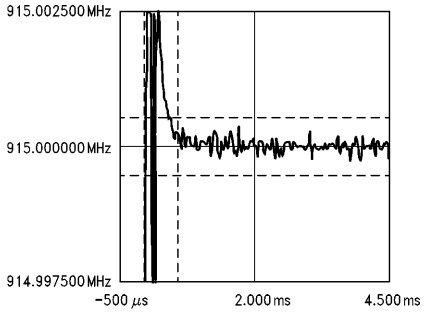

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FIGURE 12. PLL Frequency Jump Lock Time

APPENDIX

Derivation of ωc

The impedance of the loop filter shown in *Figure 5* is

$$Z_T(s) = \frac{Z(s) \bullet \left(\frac{1}{s\,C3}\right)}{Z(s) + R3 + \left(\frac{1}{s\,C3}\right)} \tag{19}$$

where Z(s) is given by equation 1.

Knowing that $C1 \geq 10\,C3;$

and by substituting $T3 = R3 \bullet C3$

along with equations 2a, 2b.

simplifies the third order equation for the open loop gain to

$$G(s) \bullet H(s)\Big|_{s = j\bullet\omega} = \frac{-Kpd \bullet Kvco\,(1 + j\omega \bullet T2)}{\omega^2\,C1 \bullet N\,(1 + j\omega \bullet T1)} \bullet \frac{T1}{T2} \bullet \frac{1}{(1 + j\omega \bullet T3)} \tag{20}$$

$$\phi(\omega) \propto (1 + \omega \bullet T2) \bullet (1 - \omega \bullet T1) \bullet (1 - \omega \bullet T3) \tag{21}$$

Similar to equation 9

$$T2 = \frac{1}{\omega^2\,(T1 + T3)} \tag{22}$$

Substituting (22) into (21) gives

$$\phi(\omega) \propto 2 - \omega^2 \bullet T1 \bullet T3 - j\omega \bullet (T1 + T3) + \frac{j}{\omega \bullet (T1 + T3)} - \frac{j\omega \bullet T1 \bullet T3}{(T1 + T3)} \tag{23}$$

Thus

$$\tan\phi = \frac{-\omega \bullet (T1 + T3) - \dfrac{\omega \bullet T1 \bullet T3}{(T1 + T3)} + \dfrac{1}{\omega \bullet (T1 + T3)}}{2 - \omega^2 \bullet T1 \bullet T3} \tag{24}$$

Assuming $\omega^2 \bullet T1 \bullet T2 \ll 2$ (25)

After some manipulation we arrive at the characteristic equation

$$\omega^2 + \omega\,\frac{2\tan\phi \bullet (T1 + T2)}{[(T1 + T3)^2 + T1 \bullet T3]} - \frac{1}{(T1 + T3)^2 + T1 \bullet T3} = 0 \tag{26}$$

Taking the negative root, and multiplying through gives the expression for the closed loop bandwidth, ω_C, equation (20).

$$\omega_C = \frac{\tan\phi \bullet (T1 + T3)}{[(T1 + T3)^2 + T1 \bullet T3]} \bullet \left[\sqrt{1 + \frac{(T1 + T3)^2 + T1 \bullet T3}{[\tan\phi \bullet (T1 + T3)]^2}} - 1\right]$$

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